



# Cannon / Coffee / Whiskey Lake-LP Client Platform

SPI Programming Guide

January 2019

Revision 1.9

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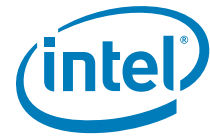
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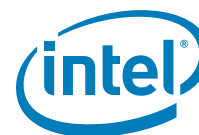
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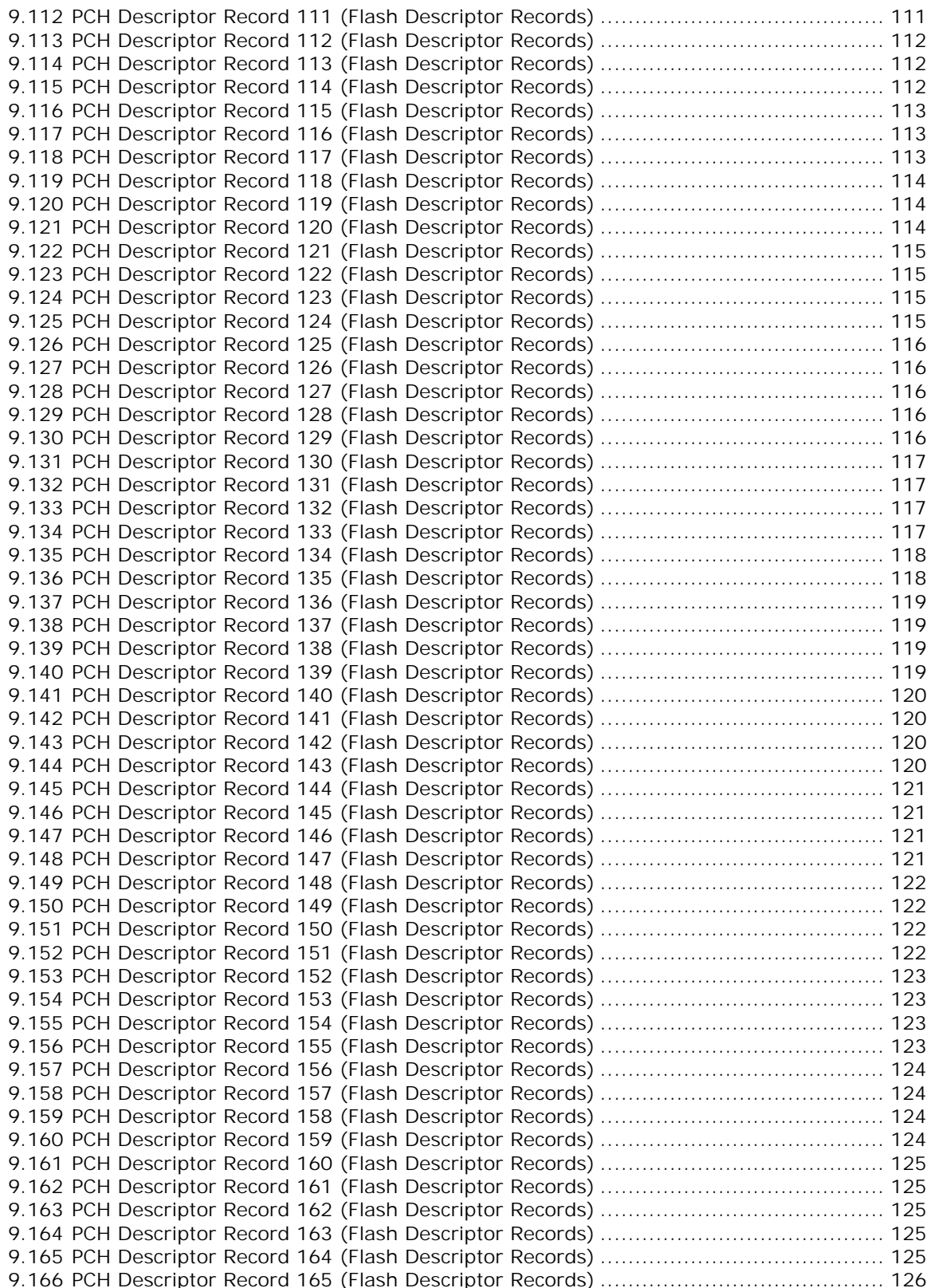
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## Revision History

Document Number	Revision Number	Description	Revision Date
	0.8	<ul style="list-style-type: none"><li>Initial Release - Harness version v134</li></ul>	May 2017
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	1.5	<ul style="list-style-type: none"><li>Updated SMLink1 GP Target and SMLink1 I<sup>2</sup>C* Target usage information</li></ul>	June 2018
	1.6	<ul style="list-style-type: none"><li>New Delayed Authentication Mode strap setting added to 0xC40</li></ul>	August 2018
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	1.8	<ul style="list-style-type: none"><li>Updated offset 0x144 bit 2 default value</li></ul>	November 2018
	1.9	<ul style="list-style-type: none"><li>Updated Platform IMON setting information</li></ul>	January 2019

§ §



# 1 Introduction

## 1.1 Overview

This manual is intended for OEMs and software vendors to clarify various aspects of programming the SPI flash on PCH family based platforms. The current scope of this document is for Intel® microarchitecture code name Cannonlake PCH-LP only.

### [Chapter 2, "PCH SPI Flash Architecture"](#)

- Overview of SPI flash, Descriptor, Flash Layout, compatible SPI flash.

### [Chapter 3, "PCH SPI Flash Compatibility Requirement"](#)

- Overview of compatibility requirements for **Cannonlake PCH-LP** products.

### [Chapter 4, "Descriptor Overview"](#)

- Overview of the descriptor and Descriptor record definition

### [Chapter 5, "Serial Flash Discoverable Parameter \(SFDP\) Overview"](#)

- Overview of the SFDP definition.

### [Chapter 6, "Configuring BIOS/GbE for SPI Flash Access"](#)

- Describes how to configure BIOS/GbE for SPI flash access.

### [Chapter 7, "IFWI / Intel® ME Disable for Debug/Flash Burning Purposes"](#)

- Methods of disabling Intel Management Engine for debug purposes.

### [Chapter 8, "Recommendations for SPI Flash Programming in Manufacturing Environments"](#)

- Recommendations for manufacturing environments.

### [Chapter 9, "Flash Descriptor PCH / PMC / CPU and Intel® ME Configuration Section"](#)

- Flash Descriptor PCH / CPU Soft Strap Section.

### [Chapter 10, "Configuration Dependencies"](#)

- Descriptor configuration dependencies for enabling Cannonlake Hardware I/O, Bus and GPIO components.

### [Appendix A, "FAQ and Troubleshooting"](#)

- Frequently asked questions and Troubleshooting tips.



## 1.2 Terminology

Table 1-1. Terminology

Term	Description
BIOS	Basic Input-Output System
CRB	Customer Reference Board
Intel® FPT	Intel® Flash Programming Tool - programs the SPI flash
FIT	Intel® Flash Image Tool – creates a flash image from separate binaries
FW	Firmware
FWH	Firmware Hub – LPC based flash where BIOS may reside
GbE	Intel® Integrated 1000/100/10
HDCP	High-bandwidth Digital Content Protection
IFWI	Integrated Firmware Image Layout
Intel® AMT	Intel® Active Management Technology
Cannonlake PCH-LP	Cannonlake Platform Integrated I/O
Intel® Management Engine Firmware (Intel® ME FW)	Intel firmware that adds Intel® Active Management Technology, Castle Peak, Sentry Peak, etc.
Intel PCH	Intel® Platform Controller Hub
Intel PCHn family	All PCHn derivatives including PCHn (desktop) and PCHnM (mobile)
LPC	Low Pin Count Bus- bus on where legacy devices such a FWH reside
LVSCC	Lower Vendor Specific Component Capabilities
MCP	Multi-Chip package
MDTBA	MIP Descriptor Table Base Address
MIP	Master Image Profile
PCH	Platform Controller Hub
PCH-LP	Platform Controller Hub – Low Power
PMC	Power Management Controller (PCH)
SFDP	Serial Flash Discoverable Parameter
SPI	Serial Peripheral Interface – refers to serial flash memory in this document
UVSCC	Upper Vendor Specific Component Capabilities
VSCC	Vendor Specific Component Capabilities

## 1.3 Reference Documents

Table 1-2. Reference Documents

Document	Document # / Location
<i>Cannonlake PCH- LP External Design Specification (EDS)</i>	Contact your Intel field representative.
<i>Intel® Flash Image Tool (FIT)</i>	\\System Tools\\Flash Image Tool of latest Intel® ME kit from VIP. The Kit MUST match the platform you intend to use the flash tools for.
<i>Intel® Flash Programming Tool (FPT)</i>	\\System Tools\\Flash Programming Tool of latest Intel® ME from VIP. The Kit MUST match the platform you intend to use the flash tools for.



Table 1-2. Reference Documents

Document	Document # / Location
<i>FW Bring Up Guide</i>	Root directory of latest Intel® Management Engine kit from VIP. The Kit MUST match the platform you intend to use the flash tools for.

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## 2 PCH SPI Flash Architecture

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### 2.1 Descriptor Mode

The Cannonlake Platform supports up to two SPI flash devices. The flash connected to Chip Select 0 must contain a valid Descriptor as defined in Section 4. The contents of the Descriptor provide platform configuration and enable the PCH to securely manage storage among multiple users/purposes.

SPI flash must be connected directly to the PCH SPI bus.

**Note:** Cannonlake only supports Descriptor mode.

See ***SPI Supported Feature Overview*** of the latest Intel Platform Controller Hub Family External Design Specification (EDS) for Cannonlake PCH Family for more detailed information.

### 2.2 Serial Flash Discoverable Parameter (SFDP)

Serial flash with SFDP have their supported capabilities and commands stored inside the serial flash devices. The controller will discover the attributes needed to operate.

Cannonlake PCH requires SPI flash devices support JEDEC standard JESD216 SDFDP (Serial Flash Discoverable Parameters. Revision A (JESD216A) or later is strongly recommended but not mandatory. SFDP provides a consistent method of describing the functional and feature capabilities of SPI devices in a standard set of internal parameter tables. These parameter tables can be interrogated by PCH to enable adjustment needed to accommodate divergent feature from multiple vendors.

Please refer to [Chapter 5, “Serial Flash Discoverable Parameter \(SFDP\) Overview”](#) for more information.

### 2.3 SPI Fast Read

**Note:** See ***SPI for Flash*** section of the latest Intel Platform Controller Hub Family External Design Specification (EDS) for Cannonlake PCH Family for more detailed information. 60-MHz support requires SPI component that meet 66-MHz timing.

### 2.4 Intel® Trusted Platform Module (Intel® TPM) on SPI Bus

Cannonlake PCH-LP Family supports Intel TPM on the SPI bus.

See ***Serial Peripheral Interface (SPI)*** section of the latest Intel Platform Controller Hub Family External Design Specification (EDS) for Cannonlake PCH Family for more detailed information.

### 2.5 Boot Flow for Cannonlake PCH-LP Family

See Boot BIOS strap in the **Functional Straps** of the latest Intel Platform Controller Hub Family External Design Specification (EDS) for Cannonlake PCH Family for more detailed information.



See [Chapter 4, “Descriptor Overview”](#) for more detailed information.

## 2.6 Flash Regions

The controller can divide the SPI flash into separate regions below.

Region	Content
0	Descriptor
1	BIOS
2	IFWI (Integrated Firmware Image) <sup>1</sup>
3	GbE – Location for Integrated LAN firmware and MAC address
4	PDR – Platform Data Region (Optional) <sup>2</sup>
8	EC - Embedded Controller (Optional) <sup>3</sup>

**Notes:**

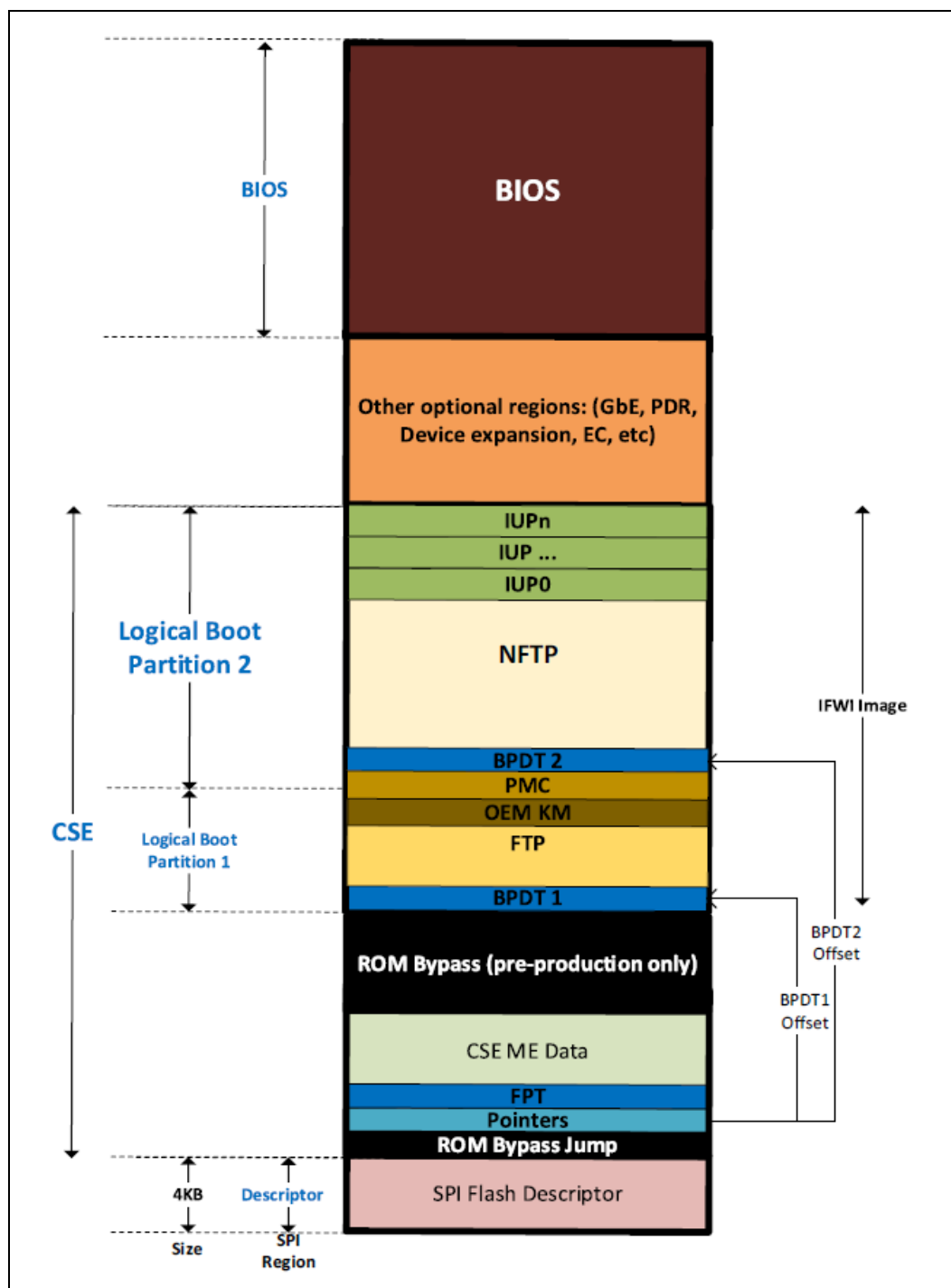
1. Also include as a part of IFWI in some instances is Intel® Management Engine (Intel® ME FW) ROM Bypass
2. The PDR region is optional and is not applicable for Cannonlake PCH-LP or not required for proper platform operation.
3. The EC region is optional and is not required for proper platform operation.

See ***SPI Flash Regions*** section of the latest Intel Platform Controller Hub Family External Design Specification (EDS) for Cannonlake PCH-LP Family for more detailed information.

### 2.6.1 Flash Region Layout

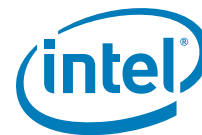
In the SPI Controller; a 4K descriptor at the base of the SPI device splits the device into regions and defines the access control to each region.

Figure 2-1. SPI Flash Region Layout



As seen in Figure 2-1, the descriptor defines at least the following device regions:

1. **Intel® ME ROM Bypass Region:** Starting from offset 4K. This region is used for Intel® ME ROM Bypass. When Intel® ME ROM Bypass does not exist, this region size is 0.
2. **IFWI Region:** This region starts after the Intel® ME ROM Bypass region.
3. **BIOS Region:** This region starts after the IFWI region.



## 2.6.2 Flash Region Sizes

SPI flash space requirements differ by platform and configuration. Please refer to documentation specific to your platform for BIOS and ME Region flash size estimates.

See ***SPI Flash Regions*** section of the latest *Intel Platform Controller Hub Family External Design Specification (EDS)* for Cannonlake PCH-LP Family for more detailed information.

## 2.7 Hardware Sequencing

Host/Bios and ME may read/write /erase flash via Hardware Sequencing or Software Sequencing registers.

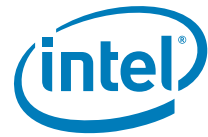
Cannonlake Hardware sequencing has been enhanced to include all operations the BIOS needs to perform.

**Note:** Host / Bios Software Sequencing is not supported in Cannonlake.

Hardware sequencing has a predefined list of opcodes, the PCH discovers the 4k and 64k erase opcodes via SFDP.

See ***Serial Peripheral Interface Memory Mapped Configuration Registers*** in *Cannonlake PCH-LP Family External Design Specification (EDS)* for more details.

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## 3 PCH SPI Flash Compatibility Requirement

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### 3.1 Cannonlake PCH SPI Flash Requirements

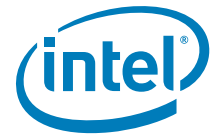
- Cannonlake PCH Family allows for up to two SPI flash devices to store BIOS, Intel® ME FW and integrated LAN information.
  - **Intel® ME FW is required for Cannonlake PCH Family-based platforms**
  - Each SPI component can support up to 64 MB (128 MB total addressable) using 26-bit addressing
- 3.3V or 1.8V SPI I/O buffer VCC
- SPI Fast Read instruction is supported at of 17 MHz, 30 MHz and 48 MHz frequencies.
- SPI Dual Output and Dual I/O Fast Read instruction is supported at frequencies of 17 MHz, 30 MHz and 48 MHz.
- SPI Quad Output and Quad I/O Fast read instruction is supported at frequencies of 17 MHz, 30 MHz and 48 MHz.

If there are two SPI components, both components have to support fast read in order to enable Fast Read in PCH.

Enabling Quad mode reads may require special configuration of the flash device during platform manufacturing, prior to first boot. No special configuration is required for flash devices that support Quad mode but do not contain a Quad Enable (QE) bit. Flash devices that contain a QE bit must be configured with QE=1. Several manufacturers offer SKU's with QE=1 by default.

#### 3.1.1 General Requirements

- Erase size capability of: 4 KBytes erase must be supported uniformly across the flash array. If 64k erase is also supported, then it must be supported uniformly across the flash array.
- Serial flash device must ignore the upper address bits such that an address of FFFFFFFh aliases to the top of the flash memory.
- SPI Compatible Mode 0 support: Clock phase is 0 and data is latched on the rising edge of the clock.
- If the device receives a command that is not supported or incomplete (less than 8 bits), the device must discard the cycle gracefully without any impact on the flash content.
- An erase command (page, sector, block, chip, etc.) must set all bits inside the designated area (page, sector, block, chip, etc.) to 1 (Fh).
- Status Register bit 0 must be set to 1 when a write, erase or write to status register is in progress and cleared to 0 when a write or erase is NOT in progress.
- Devices requiring the Write Enable command must automatically clear the Write Enable Latch at the end of Data Program instructions.



- The flexibility to perform a write between 1 byte to 64 bytes is required.
- SFDP fields: dword 1, bit 4 "Write Enable Instruction". Dword 1, bit 3 "Volatile Status Register", both bits must be 0.

Intel Management Firmware must meet the SPI flash based BIOS Requirements plus:

- [2.2 Serial Flash Discoverable Parameter \(SFDP\)](#)
- [3.1.4 JEDEC ID \(Opcode 9Fh\)](#)
- [3.1.5 Multiple Page Write Usage Model](#)
- [3.1.6 Hardware Sequencing Requirements](#)

Write protection scheme must meet guidelines as defined in [SPI Flash Unlocking Requirements for Intel Management Engine](#).

SPI Flash Unlocking Requirements for Intel Management Engine

- a. Flash devices must be globally unlocked (read, write and erase access on the ME region) from power on by writing 0 to the Block Protect bits in the flash's status register to disable write protection.
- b. If the status register must be unprotected, it must use the write enable 06h instruction.
- c. Opcode 01h (write to status register) must then be used to write 0 to the Block Protect bits in the status register. If the device contains a Quad Enable bit in the status register, then firmware must perform a read-modify-write to prevent changing the state of the QE bit when writing to the status register. This must unlock the entire part. If the SPI flash's status register has non-volatile bits that must be written to, bits [5:2] of the flash's status register must be all 0h to indicate that the flash is unlocked.

### 3.1.2 Bios Requirement

BIOS must ensure there is no SPI flash based read/write/erase protection on the GbE region. GbE firmware and drivers for the integrated LAN need to be able to read, write and erase the GbE region at all times.

### 3.1.3 Software / Firmware Requirements

The recommended Intel ME firmware flow for clearing block protect is:

1. Determine the location of the Quad Enable (QE) bit using the SFDP table QER field (for devices that support SFDP rev A or later) or the VSCC table QER field (for SDFDP rev -)
2. Read status registers 1 and 2.
3. Modify status to clear Block Protect bits and leave QE bit unchanged.
4. Write the status register using an atomic {write\_enable, write\_status} sequence (this happens automatically when hardware sequencing is used).
5. Issue a write\_disable instruction using software sequencing.

After global unlock, BIOS has the ability to lock down small sections of the flash as long as they do not involve the ME or GbE region. See [6.1 Unlocking SPI Flash Device Protection for Cannonlake PCH-LP Platform](#) and [6.2 Locking SPI Flash via Status Register](#) for more information about flash based write/erase protection.



### 3.1.4 JEDEC ID (Opcode 9Fh)

Since each serial flash device may have unique capabilities and commands, the JEDEC ID is the necessary mechanism for identifying the device so the uniqueness of the device can be comprehended by the controller (master). The JEDEC ID uses the opcode 9Fh and a specified implementation and usage model. This JEDEC Standard Manufacturer and Device ID read method is defined in Standard JESD21-C, PRN03-NV1 and is available on the JEDEC website: [www.jedec.org](http://www.jedec.org).

### 3.1.5 Multiple Page Write Usage Model

Intel platforms have firmware usage models which require that the serial flash device support multiple writes to a page (minimum of 512 writes) without requiring a preceding erase command. BIOS commonly uses capabilities such as counters that are used for error logging and system boot progress logging. These counters are typically implemented by using byte-writes to 'increment' the bits within a page that have been designated as the counter. The Intel firmware usage models require the capability for multiple data updates within any given page. These data updates occur via byte-writes without executing a preceding erase to the given page. Both the BIOS and Intel Management Engine firmware multiple page write usage models apply to sequential and non-sequential data writes.

Flash parts must also support the writing of a single byte 1024 times in a single 256-byte page without erase. There will be 64 pages where this usage model will occur. These 64 pages will be every 16 kilobytes.

### 3.1.6 Hardware Sequencing Requirements

The following table contains a list of commands and the associated opcodes that a SPI-based serial flash device must support in order to be compatible with hardware sequencing.

Commands	OPCODE	Notes
Write to Status Register	01h	Writes a byte to SPI flash's status register. Enable Write to Status Register command must be run prior to this command
Program Data	02h	Single byte or 64 byte write as determined by flash part capabilities and software
Read Data	03h	
Write Disable	04h	
Read Status	05h	Outputs contents of SPI flash's status register
Write Enable	06h	
Fast Read	0Bh	
Enable Write to Status Register	06h	If write-status 01h requires a write-enable, then 06h must enable write-status.
Erase	Programmable/ Discoverable	4 Kbyte erase. Uses the value from SFDP (if available) else value from VSCCn Erase Opcode register value
Chip Erase	C7h and/or 60	
JEDEC ID	9Fh	<a href="#">See Section 3.1.4 for more information</a>
Dual Output Fast Read	3Bh/ Discoverable	Discoverable opcodes are obtained from each component's SFDP table
Dual I/O Fast Read	Discoverable	Opcode is obtained from each component's SFDP table
Quad I/O Fast Read	Discoverable	Opcode is obtained from each component's SFDP table





## 3.2 Cannonlake PCH SPI AC Electrical Compatibility Guidelines

Table 3-1. SPI Timings (17 MHz)

Sym	Parameter	Min	Max	Units	Notes
t180a	Serial Clock Frequency - 17MHz Operation	17.06	18.73	MHz	1
t183a	Tco of SPI_MOSI with respect to serial clock falling edge at the host	-5	13	ns	
t184a	Setup of SPI_MISO with respect to serial clock falling edge at the host	16	-	ns	
t185a	Hold of SPI_MISO with respect to serial clock falling edge at the host	0	-	ns	
t186a	Setup of SPI_CS[1:0]# assertion with respect to serial clock rising edge at the host	30	-	ns	
t187a	Hold of SPI_CS[1:0]# assertion with respect to serial clock rising edge at the host	30	-	ns	
t188a	SPI_CLK High time	26.37	-	ns	2
t189a	SPI_CLK Low time	26.82	-	ns	2
<b>Notes:</b> 1. Typical clock frequency driven by Cannonlake PCH Family is 17.86 MHz. 2. Measurement point for low time and high time is taken at 0.5(VccSPI).					

Table 3-2. SPI Timings (30 MHz)

Sym	Parameter	Min	Max	Units	Notes
t180b	Serial Clock Frequency - 30MHz Operation	29.83	32.81	MHz	1
t183b	Tco of SPI_MOSI with respect to serial clock falling edge at the host	-5	5	ns	
t184b	Setup of SPI_MISO with respect to serial clock falling edge at the host	8	-	ns	
t185b	Hold of SPI_MISO with respect to serial clock falling edge at the host	0	-	ns	
t186b	Setup of SPI_CS[1:0]# assertion with respect to serial clock rising edge at the host	30	-	ns	
t187b	Hold of SPI_CS[1:0]# assertion with respect to serial clock rising edge at the host	30	-	ns	
t188b	SPI_CLK High time	14.88	-	ns	2
t189b	SPI_CLK Low time	15.18	-	ns	2
<b>Notes:</b> 1. Typical clock frequency driven by Cannonlake PCH Family is 30 MHz. 2. Measurement point for low time and high time is taken at 0.5(VccSPI).					



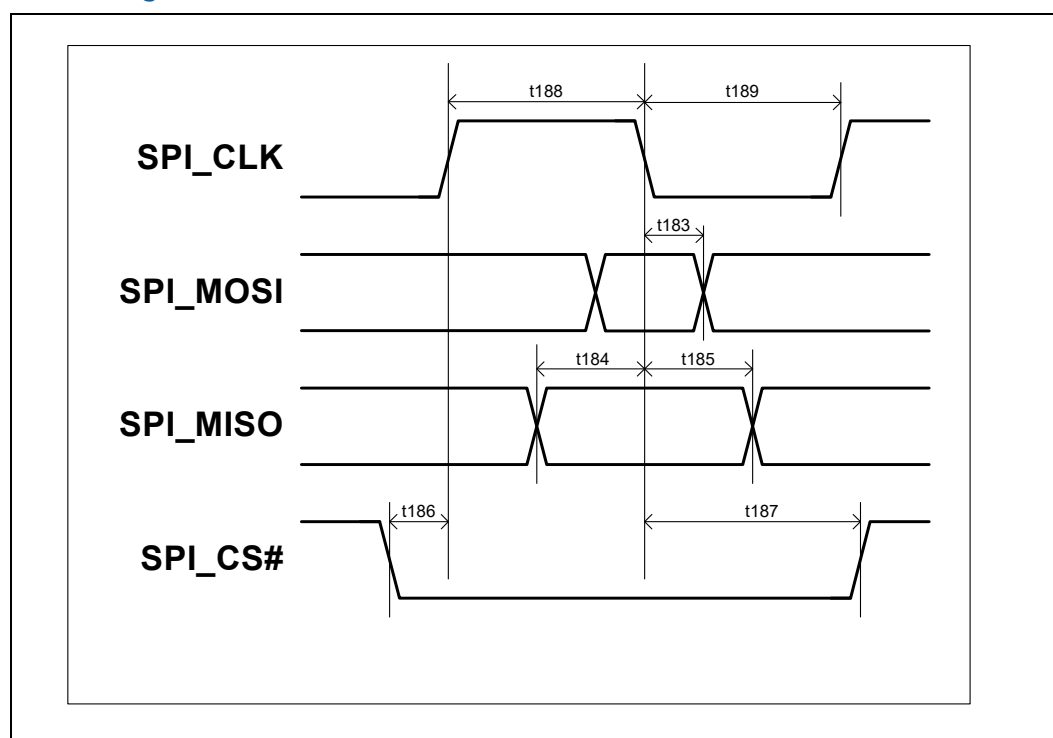
Table 3-3. SPI Timings (48 MHz)

Sym	Parameter	Min	Max	Units	Notes
t180c	Serial Clock Frequency - 48 MHz Operation	46.99	53.40	MHz	1
t183c	Tco of SPI_MOSI with respect to serial clock falling edge at the host	-3	3	ns	
t184c	Setup of SPI_MISO with respect to serial clock falling edge at the host	8	-	ns	
t185c	Hold of SPI_MISO with respect to serial clock falling edge at the host	0	-	ns	
t186c	Setup of SPI_CS[1:0]# assertion with respect to serial clock rising edge at the host	30	-	ns	
t187c	Hold of SPI_CS[1:0]# assertion with respect to serial clock rising edge at the host	30	-	ns	
t188c	SPI_CLK High time	7.84	-	ns	2, 3
t189c	SPI_CLK Low time	11.84	-	ns	2, 3

**Notes:**

1. Typical clock frequency driven by Cannonlake PCH Family is 48 MHz.
2. When using 48 MHz mode ensure target flash component can meet t188c and t189c specifications. Measurement should be taken at a point as close as possible to the package pin.
3. Measurement point for low time and high time is taken at 0.5(VccSPI).

Figure 3-1. SPI Timing

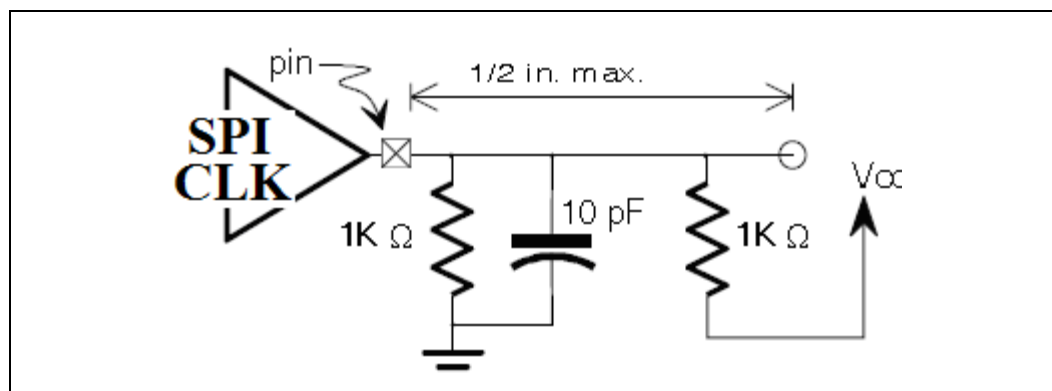


### 3.3 SPI Flash DC Electrical Compatibility Guidelines

Parameter	Min	Max	Units	Notes
Supply Voltage (Vcc)	3.14	3.7	V	
Input High Voltage	$0.5 \cdot V_{CC}$	$V_{CC} + 0.5$	V	
Input Low Voltage	-0.5	$0.3 \cdot V_{CC}$	V	
Output High Characteristics	$0.9 \cdot V_{CC}$	$V_{CC}$	V	$I_{oh} = -0.5\text{mA}$
Output Low Characteristics		$0.1 \cdot V_{CC}$		$I_{ol} = 1.5\text{mA}$
Input Leakage Current	-10	10	$\mu\text{A}$	
Output Rise Slew Rate (0.2 Vcc - 0.6 Vcc)	1	4	V/ns	1
Output Fall Slew Rate (0.6 Vcc - 0.2 Vcc)	1	4	V/ns	1

**Note:**  
 1. Testing condition: 1K pull up to Vcc, 1kohm pull down and 10 pF pull down and 1/2 inch trace. See Figure 3.3 for more detail.

Figure 3-2. PCH Test Load



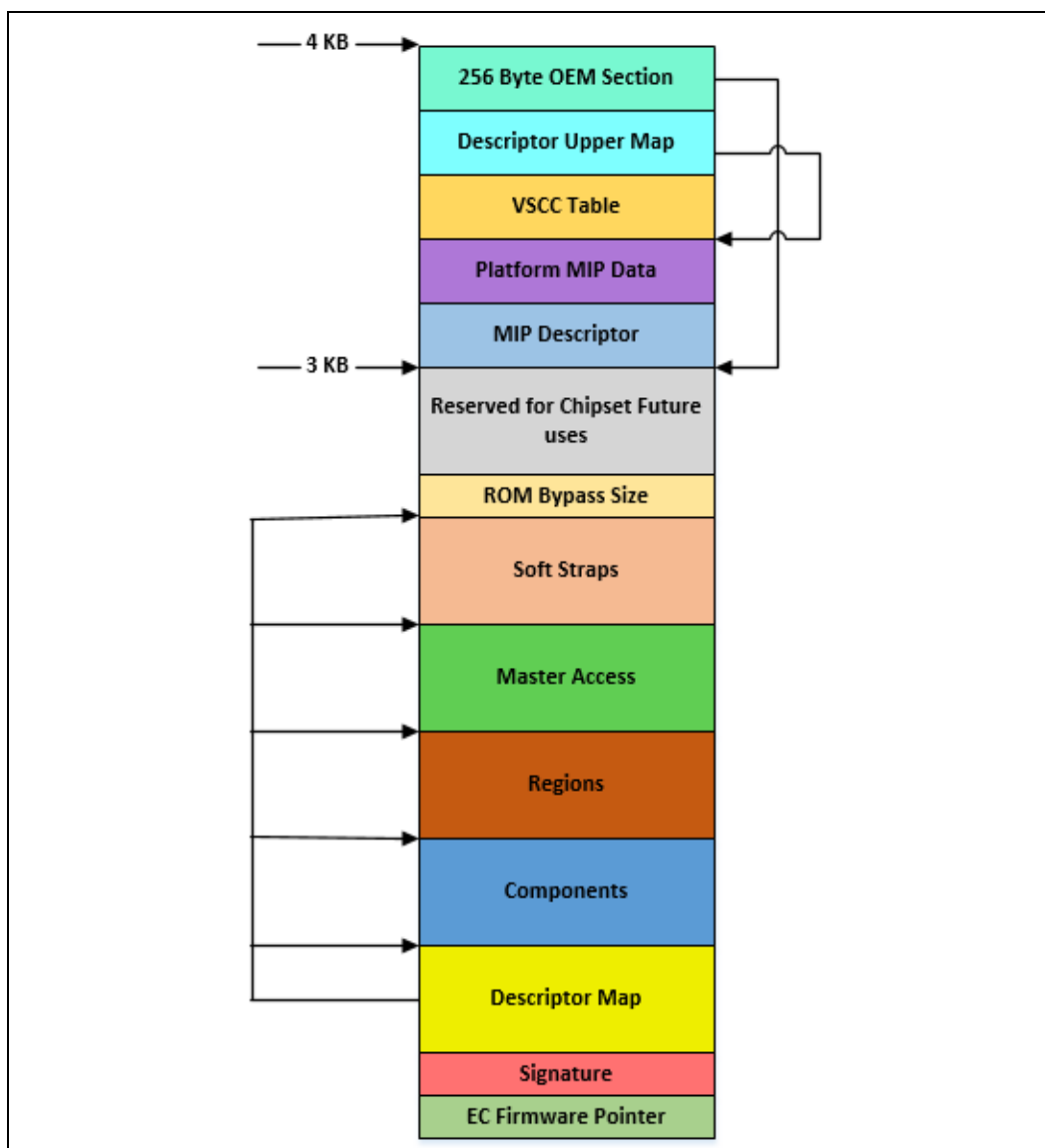
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## 4 Descriptor Overview

The Flash Descriptor is a data structure that is programmed on the SPI flash part on Cannonlake PCH based platforms. The Descriptor data structure describes the layout of the flash as well as defining configuration parameters for the PCH. The descriptor is on the SPI flash itself and is not in memory mapped space like PCH programming registers. The maximum size of the Flash Descriptor is 4 KBytes. It requires its own discrete erase block, so it may need greater than 4 KBytes of flash space depending on the flash architecture that is on the target system.

The information stored in the Flash Descriptor can only be written during the manufacturing process as its read/write permissions must be set to Read Only when the computer leaves the manufacturing floor.

Figure 4-1. Flash Descriptor (Cannonlake PCH-LP)





- EC Firmware Pointer is located in the first 16 bit of the Descriptor and contains the address location for EC flash region. The format for the EC Firmware Pointer address is dependent on EC vendors/OEM implementation of this field.
- The Flash signature at the bottom of the flash (offset 10h) must be 0FF0A55Ah in order to be in Descriptor mode.
- The Descriptor map has pointers to the lower five descriptor sections as well as the size of each.
- The Component section has information about the SPI flash part(s) the system. It includes the number of components, density of each component, read, write and erase frequencies and invalid instructions.
- The Region section defines the base and the limit of the BIOS, IFWI, GbE, PDR (Optional), Embedded Controller (EC), and Device Expansion (Intel® ME Data) regions as well as their size.
- The master region contains the hardware security settings for the flash, granting read/write permissions for each region and identifying each master.
- PCH chipset soft strap sections contain PCH configurable parameters.
- The Reserved region is for future chipset usage.
- The Descriptor Upper Map determines the length and base address of the Intel® ME VSCC Table.
- The Intel® ME VSCC Table holds the JEDEC ID and the ME VSCC information for all the SPI Flash part(s) supported by the NVM image. BIOS and GbE write and erase capabilities depend on VSCC0 and VSCC1 registers in SPIBAR memory space.
- OEM Section is 256 Byte section reserved at the top of the Flash Descriptor for use by the OEM.

See **SPI Supported Feature Overview** and **Flash Descriptor Records** in the *Cannonlake PCH-LP Family External Design Specification (EDS)*.

## 4.1 Flash Descriptor Content

The following sections describe the data structure of the Flash Descriptor on the SPI device. These are not registers or memory space within PCH. FDBAR - is address 0x0 on the SPI flash device on chip select 0.

Recommended flash descriptor map:

Region Name	Starting Address
Signature	0x10
Component FCBA	0x30
Regions FRBA	0x40
Masters FMBA	0x80
PCH Straps FPSBA	0x100
Legacy CPU Straps <sup>1</sup>	0x300
MDTBA	0xC00
PMC Straps	0xC14
CPU Straps	0xC2C
Intel® ME Straps	0xC3C
Register Init FIBA	0x340
1. The Legacy CPU Straps are for BIOS compatibility and are a duplication of the CPU Straps located 0xC30.	



## 4.1.1 Descriptor Signature and Map

### 4.1.1.1 FLVALSIG - Flash Valid Signature (Flash Descriptor Records)

Memory Address: FDBAR + 010h

Size: 32 bits

Recommended Value: 0FF0A55Ah

Bits	Description	FIT Visible
31:0	<b>Flash Valid Signature.</b> This field identifies the Flash Descriptor sector as valid. If the contents at this location contains 0FF0A55Ah, then the Flash Descriptor is considered valid and it will operate in Descriptor Mode ( <b>Note:</b> Non-Descriptor mode is not supported).	No

### 4.1.1.2 FLMAP0 - Flash Map 0 Register (Flash Descriptor Records)

Memory Address: FDBAR + 014h

Size: 32 bits

Bits	Description	FIT Visible
31:27	<b>Reserved</b>	No
26:24	<b>Reserved</b>	No
23:16	<b>Flash Region Base Address (FRBA).</b> This identifies address bits [11:4] for the Region portion of the Flash Descriptor. Bits [24:12] and bits [3:0] are 0.  Set this value to 04h. This will define FRBA as 40h.	No
15:12	<b>Reserved</b>	No
11	<b>Touch on dedicated SPI bus</b>  0 = No Touch device is connected to the dedicated Touch SPI bus 1 = Touch device is connected to the dedicated Touch SPI bus  <b>Note:</b> Hardware does not use this field. This value must be read directly from flash. It's not available via Host FDOC/FDOD registers.	Yes
10	<b>Touch on shared flash/TPM SPI bus</b>  0 = No Touch device is connected to CS1 1 = Touch device is connected to CS1 and acting as a flash device  <b>Note:</b> Hardware does not use this field. This value must be read directly from flash. It's not available via Host FDOC/FDOD registers.	Yes
9:8	<b>Number Of Components (NC).</b> This field identifies the total number of Flash Components. Each supported Flash Component requires a separate chip select. 00 = 1 Component 01 = 2 Components All other settings = Reserved  <b>Note:</b> With the introduction of DnX mode support, the flash controller ignores this descriptor field. It determines the number of attached flash components by virtue of SFDP discovery. Software may still use this field, therefore it must be properly initialized.	Yes



Bits	Description	FIT Visible
7:0	<b>Flash Component Base Address (FCBA)</b> . This identifies address bits [11:4] for the Component portion of the Flash Descriptor. Bits [24:12] and bits [3:0] are 0.  set this field to 03h. This will define FCBA as 30h	No





#### 4.1.1.3 FLMAP1 - Flash Map 1 Register (Flash Descriptor Records)

Memory Address: FDBAR + 018h

Size: 32 bits

Bits	Description	FIT Visible
31:24	<b>PCH Strap Length (PSL)</b> . Identifies the 1s based number of Dwords of PCH Straps to be read, up to 255 DWs (1KB) max. A setting of all 0's indicates there are no PCH DW straps.  This field <b>MUST</b> be set to 45h	No
23:16	<b>Flash PCH Strap Base Address (FPSBA)</b> . This identifies address bits [11:4] for the PCH Strap portion of the Flash Descriptor. Bits [24:12] and bits [3:0] are 0.  Set this field to 10h. This will define FPSBA to 100h	No
15:11	Reserved	No
10:8	<b>Number Of Masters (NM)</b> . This field identifies the total number of Flash Masters.  <b>Note:</b> This field is not used by the Flash Controller.	No
7:0	<b>Flash Master Base Address (FMBA)</b> . This identifies address bits [11:4] for the Master portion of the Flash Descriptor. Bits [24:12] and bits [3:0] are 0.  Set this field to 08h. This will define FMBA as 80h	No

#### 4.1.1.4 FLMAP2—Flash Map 2 Register (Flash Descriptor Records)

Memory Address: FDBAR + 01Ch

Size: 32 bits

Bits	Description	FIT Visible
31:24	<b>Register Init Length (RIL)</b> : Identifies the 1's based number of register initialization entries. If this field is set to 0, then there are no Register Init entries to send. Each register init entry is 2DW in length. Set this field to 0h.	No
23:16	Reserved. Set this field to 34h.	No
15:0	Reserved	No



## 4.1.2 Flash Descriptor Component Section

### 4.1.2.1 FLCOMP—Flash Components Register (Flash Descriptor Records)

The following section of the Flash Descriptor is used to identify the different SPI Flash Components and their capabilities.

Memory Address: FCBA + 000h

Size: 32 bits

Bits	Description	FIT Visible
31	Reserved	No
30	<b>Dual Output Fast Read Support</b> 0 : Dual Output Fast Read is not supported 1 : Dual Output Fast Read is supported <b>Notes:</b> 1. This setting is no longer required.	No
29:27	<b>Read ID and Read Status Clock Frequency.</b> 001 = Reserved 010 = 48 MHz 100 = 30 MHz 110 = 17 MHz All other Settings = Reserved <b>Notes:</b> 1. If more than one Flash component exists, this field must be set to the lowest common frequency of the different Flash components. 2. If setting to 48, ensure flash meets timing requirements defined in <a href="#">Table 3-3</a>	Yes
26:24	<b>Write and Erase Clock Frequency.</b> 001 = Reserved 010 = 48 MHz 100 = 30 MHz 110 = 17 MHz All other Settings = Reserved <b>Notes:</b> 1. If more than one Flash component exists, this field must be set to the lowest common frequency of the different Flash components. 2. If setting to 48, ensure flash meets timing requirements defined in <a href="#">Table 3-3</a>	Yes
23:21	<b>Fast Read Clock Frequency.</b> This field identifies the frequency that can be used with the Fast Read instruction. This field is undefined if the Fast Read Support field is '0'. 001 = Reserved 010 = 48 MHz 100 = 30 MHz 110 = 17 MHz All other Settings = Reserved <b>Notes:</b> 1. If more than one Flash component exists, this field must be set to the lowest common frequency of the different Flash components. 2. If setting to 48MHz, ensure flash meets timing requirements defined in <a href="#">Table 3-3</a>	Yes



Bits	Description	FIT Visible
20	<p><b>Fast Read Support.</b>            0 = Fast Read is not Supported            1 = Fast Read is supported</p> <p>If the Fast Read Support bit is a '1' and a device issues a Direct Read or issues a read command from the Hardware Sequencer and the length is greater than 4 bytes, then the SPI Flash instruction should be "Fast Read". If the Fast Read Support is a '0' or the length is 1-4 bytes, then the SPI Flash instruction should be "Read".</p> <p>Reads to the Flash Descriptor always use the Read command independent of the setting of this bit.</p> <p><b>Notes:</b>            1. If more than one Flash component exists, this field can only be set to '1' if both components support Fast Read.            2. It is strongly recommended to set this bit to 1b</p>	Yes
19:17	<p><b>eSPI / EC Bus Frequency:</b></p> <p>For Slave 0 (EC/BMC): Indicates the maximum frequency of the eSPI bus that is supported by the eSPI Master and platform configuration (trace length, number of Slaves, etc.). The actual frequency of the eSPI bus will be the minimum of this field and the Slave's maximum frequency advertised in its General Capabilities register.</p> <p>0x0 = 20MHz            0x1 = 24MHz            0x2 = 30 MHz            0x3 = 48MHz            0x4 = 60MHz            05x = Reserved            0x6 = Reserved            0x7 = Reserved</p>	Yes
16	Reserved	No
15	<p><b>Quad I/O Read Enable (QIORE):</b>            0 = Quad I/O Read is disabled            1 = Quad I/O Read is enabled</p> <p>This soft strap only has effect if Quad Output Read is discovered as supported via the SFDP            If parameter table is not detected via SFDP, this bit has no effect and Quad I/O Read is controlled via the Flash Descriptor Component Section.</p>	Yes
14	<p><b>Quad Output Read Enable (QORE):</b>            0 = Quad Output Read is disabled            1 = Quad Output Read is enabled</p> <p>This soft strap only has effect if Quad Output Read is discovered as supported via the SFDP            If parameter table is not detected via SFDP, this bit has no effect and Quad Output Read is controlled via the Flash Descriptor Component Section.</p>	Yes
13	<p><b>Dual I/O Read Enable (DIORE):</b>            0 = Dual I/O Read is disabled            1 = Dual I/O Read is enabled</p> <p>This soft strap only has effect if Dual I/O Read is discovered as supported via the SFDP            If parameter table is not detected via SFDP, this bit has no effect and Dual Output I/O Read is controlled via the Flash Descriptor Component Section.</p>	Yes



Bits	Description	FIT Visible
12	<b>Dual Output Read Enable (DORE):</b> 0 = Dual Output Read is disabled 1 = Dual Output Read is enabled  This soft strap only has effect if Dual Output read is discovered as supported via the SFDP. If parameter table is not detected via SFDP, this bit has no effect and Dual Output Read is controlled via the Flash Descriptor Component Section.	Yes
11:10	<b>eSPI / EC Maximum I/O Mode:</b> Indicates the maximum IO Mode (Single/Dual/Quad) of the eSPI bus that is supported by the eSPI Master and specific platform configuration. The actual IO Mode of the eSPI bus will be the minimum of this field and the Slave's maximum IO Mode advertised in its General Capabilities register.  0x0 = Single IO Mode 0x1 = Single and Dual IO Mode 0x2 = Single and Quad IO Mode 0x3 = Single, Dual and Quad I/O	Yes
9	<b>SPI Voltage Select (SPI_1p8volt_sel):</b>  0 = SPI supply voltage set to 3.3 volts 1 = SPI supply voltage set to 1.8 volts  This strap sets the internal control signal on the pad for either 1.8 or 3.3 V operation.  <b>Note:</b> The strap defaults to 1.8V mode before the soft straps are loaded, i.e. before the actual supply voltage is known. This is because the pad performance is slightly better when assuming 1.8V when the actual is 3.3V than vice-versa.	Yes
8	Reserved	No
7:4	<b>Component 1 Density. (C1DEN)</b> This field identifies the size of the 2nd Flash component connected directly to the PCH. If there is not 2nd Flash component, the contents of this field should be read as "1111b" 0000 = 512 KB 0001 = 1 MB 0010 = 2 MB 0011 = 4 MB 0100 = 8 MB 0101 = 16 MB 0110 = 32 MB 0111 = 64 MB 1000 - 1110 = Reserved  <b>Note:</b> This field is defaulted to "1111b" after reset <b>Note:</b> C1DEN field will be <b>ignored</b> if FLMAPO.NC bit [9:8] is set to 00 i.e. 1 component only.	Yes
3:0	<b>Component 0 Density (CODEN).</b> This field identifies the size of the 1st or only Flash component connected directly to the PCH. 0000 = 512 KB 0001 = 1 MB 0010 = 2 MB 0011 = 4 MB 0100 = 8 MB 0101 = 16 MB 0110 = 32 MB 0111 = 64 MB 1000 - 1111 = Reserved  <b>Note:</b> This field is defaulted to "0101b" (16MB) after reset.	Yes



#### 4.1.2.2 FLILL—Flash Invalid Instructions Register (Flash Descriptor Records)

Memory Address: FCBA + 004h

Size: 32 bits

Bits	Description	FIT Visible
31:24	<b>Invalid Instruction 3.</b> <b>Default set to 0xAD</b> See definition of Invalid Instruction 0	Yes
23:16	<b>Invalid Instruction 2.</b> <b>Default set to 0x60</b> See definition of Invalid Instruction 0	Yes
15:8	<b>Invalid Instruction 1.</b> <b>Default set to 0x42</b> See definition of Invalid Instruction 0	Yes
7:0	<b>Invalid Instruction 0.</b> <b>Default set to 0x21</b> <b>Note:</b> Opcode for an instruction that the Flash Controller should protect against, such as Chip Erase. This byte should be set to 0 if there are no invalid instructions to protect against for this field. Opcodes programmed in the Software Sequencing Opcode Menu Configuration and Prefix-Opcode Configuration are not allowed to use any of the Invalid Instructions listed in this register.	Yes

#### 4.1.2.3 FLILL1—Flash Invalid Instructions Register (Flash Descriptor Records)

Memory Address: FCBA + 008h

Size: 32 bits

Bits	Description	FIT Visible
31:24	<b>Invalid Instruction 7.</b> <b>Default set to C7</b> See definition of Invalid Instruction 0	Yes
23:16	<b>Invalid Instruction 6.</b> <b>Default set to 0xC4</b> See definition of Invalid Instruction 0	Yes
15:8	<b>Invalid Instruction 5.</b> <b>Default set to 0xB9</b> See definition of Invalid Instruction 0	Yes



Bits	Description	FIT Visible
7:0	<b>Invalid Instruction 4.</b> <b>Default set to 0xB7</b> See definition of Invalid Instruction 0	Yes

### 4.1.3 Flash Descriptor Region Section

The following section of the Flash Descriptor is used to identify the different Regions of the NVM image on the SPI flash.

Flash Regions:

- If a particular region is not using SPI Flash, the particular region should be disabled by setting the Region Base to all 1's, and the Region Limit to all 0's (base is higher than the limit)
- For each region except FLREG0, the Flash Controller must have a default Region Base of 7FFFh and the Region Limit to 0000h within the Flash Controller in case the Number of Regions specifies that a region is not used.



#### 4.1.3.1 FLREG0—Flash Region 0 (Flash Descriptor) Register (Flash Descriptor Records)

Memory Address: FRBA + 000h

Size: 32 bits

Recommended Value: 00000000h

Bits	Description	FIT Visible
31	Reserved	No
30:16	<b>Region Limit.</b> This specifies bits 26:12 of the ending address for this Region. <b>Notes:</b> <ol style="list-style-type: none"> <li>Set this field to 0b. This defines the ending address of descriptor as being FFFh.</li> <li>Region limit address Bits[11:0] are assumed to be FFFh</li> </ol>	No
15	Reserved	No
14:0	<b>Region Base.</b> This specifies address bits 26:12 for the Region Base. <b>Note:</b> Set this field to all 0s. This defines the descriptor address beginning at 0h.	No

#### 4.1.3.2 FLREG1—Flash Region 1 (BIOS) Register (Flash Descriptor Records)

Memory Address: FRBA + 004h

Size: 32 bits

Bits	Description	FIT Visible
31	Reserved	No
30:16	<b>Region Limit.</b> This specifies bits 26:12 of the ending address for this Region. <b>Notes:</b> <ol style="list-style-type: none"> <li>Must be set to 0000h if Intel® ME ROM Bypass region is unused (on Firmware hub)</li> <li>Ensure BIOS region size is a correct reflection of actual BIOS image that will be used in the platform</li> <li>Region limit address Bits[11:0] are assumed to be FFFh</li> </ol>	No
15	Reserved	No
14:0	<b>Region Base.</b> This specifies address bits 26:12 for the Region Base. <b>Note:</b> If the BIOS region is not used, the Region Base must be programmed to 7FFFh	No

#### 4.1.3.3 FLREG2—Flash Region 2 (IFWI / Intel® ME) Register (Flash Descriptor Records)

Memory Address: FRBA + 008h

Size: 32 bits

Bits	Description	FIT Visible
31	Reserved	No
30:16	<b>Region Limit.</b> This specifies bits 26:12 of the ending address for this Region. <b>Notes:</b> <ol style="list-style-type: none"> <li>Ensure size is a correct reflection of IFWI size that will be used in the platform</li> <li>Region limit address Bits[11:0] are assumed to be FFFh</li> </ol>	No
15	Reserved	No
14:0	<b>Region Base.</b> This specifies address bits 26:12 for the Region Base.	No





#### 4.1.3.4 FLREG3—Flash Region 3 (GbE) Register (Flash Descriptor Records)

Memory Address: FRBA + 00Ch

Size: 32 bits

Bits	Description	FIT Visible
31	Reserved	No
30:16	<b>Region Limit.</b> This specifies bits 26:12 of the ending address for this Region. <b>Notes:</b> <ol style="list-style-type: none"> <li>1. The maximum Region Limit is 128KB above the region base.</li> <li>2. If the GbE region is not used, the Region Limit must be programmed to 0000h</li> <li>3. Region limit address Bits[11:0] are assumed to be FFFh</li> </ol>	No
15	Reserved	No
14:0	<b>Region Base.</b> This specifies address bits 26:12 for the Region Base. <b>Note:</b> If the GbE region is not used, the Region Base must be programmed to 7FFFh	No

#### 4.1.3.5 FLREG4—Flash Region 4 (Platform Data) Register (Flash Descriptor Records)

Memory Address: FRBA + 010h

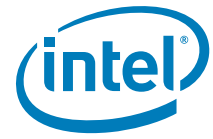
Size: 32 bits

Bits	Description	FIT Visible
31	Reserved	No
30:16	<b>Region Limit.</b> This specifies bits 26:12 of the ending address for this Region. <b>Notes:</b> <ol style="list-style-type: none"> <li>1. If PDR Region is not used, the Region Limit must be programmed to 0000h</li> <li>2. Ensure BIOS region size is a correct reflection of actual BIOS image that will be used in the platform</li> <li>3. Region limit address Bits[11:0] are assumed to be FFFh</li> </ol>	No
15	Reserved	No
14:0	<b>Region Base.</b> This specifies address bits 26:12 for the Region Base. <b>Note:</b> If the Platform Data region is not used, the Region Base must be programmed to 7FFFh	No

#### 4.1.3.6 FLREG8—Flash Region 8 (Embedded Controller) Register (Flash Descriptor Records)

Memory Address: FRBA + 020h Size: 32 bits

Bits	Description	FIT Visible
31	Reserved	No
30:16	<b>Region Limit (RL):</b> This specifies address bits 26:12 for the Region n Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREGn.Region Limit, where 7 <= n <= 11	No
15	Reserved	No
14:0	<b>Region Base.</b> This specifies address bits 26:12 for the Region Base. The value in this register is loaded from the contents in the Flash Descriptor. FLREGn.Region Base, where 7 <= n <= 11	No



**Note:** Region 6 (FRBA + 018h), Region 7 (FRBA + 01Ch) and Region 9 (FRBA + 024h), Region 10 (FRBA + 28h), Region 11 (FRBA + 2Ch), Region 12 (FRBA + 30h), Region 13 (FRBA + 34h), Region 14 (FRBA + 38h) and Region 15 (FRBA + 03Ch) are all reserved in client platform and should set to 7FFh.



## 4.1.4 Flash Descriptor Master Section

### 4.1.4.1 FLMSTR1—Flash Master 1 (Host CPU/ BIOS)

Memory Address: FMBA + 000h

Size: 32 bits

Bits	Description	FIT Visible
31:20	<b>Master Region Write Access:</b> Each bit [31:20] corresponds to Regions [11:0]. If the bit is set, this master can erase and write that particular region through register accesses. Note: Bit 21 and 26 are don't care as the primary master always has read/write permission to its primary region	Yes
19:8	<b>Master Region Read Access:</b> Each bit [19:8] corresponds to Regions [11:0]. If the bit is set, this master can read that particular region through register accesses. Note: Bit 9 and 14 are don't care as the primary master always read/write permission to its primary region.	Yes
7:4	<b>Extended Region Write Access:</b> Each bit [7:4] corresponds to Regions [15:12]. If the bit is set, this master can erase and write that particular region through register accesses.	Yes
3:0	<b>Extended Region Read Access:</b> Each bit [3:0] corresponds to Regions [15:12]. If the bit is set, this master can erase and write that particular region through register accesses.	Yes

### 4.1.4.2 FLMSTR2—Flash Master 2 (Intel® ME)

Memory Address: FMBA + 004h

Size: 32 bits

Bits	Description	FIT Visible
31:20	<b>Master Region Write Access:</b> Each bit [31:20] corresponds to Regions [11:0]. If the bit is set, this master can erase and write that particular region through register accesses. Note: Bit 22 is a don't care as the primary master always has read/write permission to its primary region	Yes
19:8	<b>Master Region Read Access:</b> Each bit [19:8] corresponds to Regions [11:0]. If the bit is set, this master can read that particular region through register accesses. Note: Bit 10 is a don't care as the primary master always read/write permission to its primary region.	Yes
7:4	<b>Extended Region Write Access:</b> Each bit [7:4] corresponds to Regions [15:12]. If the bit is set, this master can erase and write that particular region through register accesses.	Yes
3:0	<b>Extended Region Read Access:</b> Each bit [3:0] corresponds to Regions [15:12]. If the bit is set, this master can erase and write that particular region through register accesses.	Yes

### 4.1.4.3 FLMSTR3—Flash Master 3 (GbE)

Memory Address: FMBA + 008h

Size: 32 bits

Bits	Description	FIT Visible
31:20	<b>Master Region Write Access:</b> Each bit [31:20] corresponds to Regions [11:0]. If the bit is set, this master can erase and write that particular region through register accesses. Note: Bit 23 is a don't care as the primary master always has read/write permission to its primary region	Yes
19:8	<b>Master Region Read Access:</b> Each bit [19:8] corresponds to Regions [11:0]. If the bit is set, this master can read that particular region through register accesses. Note: Bit 11 is a don't care as the primary master always read/write permission to its primary region.	Yes



Bits	Description	FIT Visible
7:4	<b>Extended Region Write Access:</b> Each bit [7:4] corresponds to Regions [15:12]. If the bit is set, this master can erase and write that particular region through register accesses.	Yes
3:0	<b>Extended Region Read Access:</b> Each bit [3:0] corresponds to Regions [15:12]. If the bit is set, this master can erase and write that particular region through register accesses.	Yes

#### 4.1.4.4 FLMSTR4—Flash Master 4 (Reserved)

Memory Address: FMBA + 00Ch

Size: 32 bits

Bits	Description	FIT Visible
31:20	<b>Master Region Write Access:</b> Each bit [31:20] corresponds to Regions [11:0]. If the bit is set, this master can erase and write that particular region through register accesses. Note: Bit 17 is a don't care as the primary master always has read/write permission to its primary region	No
19:8	<b>Master Region Read Access:</b> Each bit [19:8] corresponds to Regions [11:0]. If the bit is set, this master can read that particular region through register accesses. Note: Bit 13 is a don't care as the primary master always read/write permission to its primary region.	No
7:4	<b>Extended Region Write Access:</b> Each bit [7:4] corresponds to Regions [15:12]. If the bit is set, this master can erase and write that particular region through register accesses.	No
3:0	<b>Extended Region Read Access:</b> Each bit [3:0] corresponds to Regions [15:12]. If the bit is set, this master can erase and write that particular region through register accesses.	No

#### 4.1.4.5 FLMSTR5—Flash Master 5 (EC)

Memory Address: FMBA + 010h

Size: 32 bits

Bits	Description	
31:20	<b>Master Region Write Access:</b> Each bit [31:20] corresponds to Regions [11:0]. If the bit is set, this master can erase and write that particular region through register accesses. Note: Bit 28 is a don't care as the primary master always has read/write permission to its primary region	Yes
19:8	<b>Master Region Read Access:</b> Each bit [19:8] corresponds to Regions [11:0]. If the bit is set, this master can read that particular region through register accesses. Note: Bit 16 is a don't care as the primary master always read/write permission to its primary region.	Yes
7:4	<b>Extended Region Write Access:</b> Each bit [7:4] corresponds to Regions [15:12]. If the bit is set, this master can erase and write that particular region through register accesses.	Yes
3:0	<b>Extended Region Read Access:</b> Each bit [3:0] corresponds to Regions [15:12]. If the bit is set, this master can erase and write that particular region through register accesses.	Yes



## 4.1.5 PCH / CPU Softstraps

See Chapter 9, “Flash Descriptor PCH / PMC / CPU and Intel® ME Configuration Section” for details.

## 4.1.6 Descriptor Upper Map Section

This section of the flash descriptor is used by ME to find SPI VSCC information and MIP data.

### 4.1.6.1 FLUMAP1—Flash Upper Map 1 (Flash Descriptor Records)

Memory Address: FDBAR + EFCh

Size: 32 bits

Bits	Default	Description	FIT Visible
31:24	0xC0	<b>MIP Descriptor Table Base Address (MDTBA)</b> . This identifies base address bits [11:4] for the Platform Configuration Data Structure in the Flash Descriptor Bits [26:12] and bits [3:0] are 0.  <b>Note:</b> For A Stepping parts default values is 0xC1	No
23:16	0xFF	Reserved	No
15:8	0x1	<b>Intel® ME VSCC Table Length (VTL)</b> . Identifies the 1s based number of DWORDS contained in the VSCC Table. Each SPI component entry in the table is 2 DWORDS long. Max recommended is 10 entries to allow for room for Platform Configuration Data (MIP)	No
7:0	0x1	<b>Intel® ME VSCC Table Base Address (VTBA)</b> . This identifies address bits [11:4] for the VSCC Table portion of the Flash Descriptor. Bits [26:12] and bits [3:0] are 0.	No

### 4.1.6.2 MIP - Descriptor Table

Memory Address: FDBAR + MDTBA

Name	Offset	Size (bytes)	Description	FIT Visible
Number of Descriptors	0x0	2	Number of MIP blocks ('n') inside this MIP structure	Yes
Size of MIP	0x2	2	Size, in bytes, of this MIP structure (including the MDT structure)	Yes
Block 0 Type	0x4	2	Type of block 0. Can be one of the following: 0 = CSE (USB 2 PHY Configuration) 1 = PMC Soft Straps 2 = Reserved  <b>Note:</b> In order to simplify handling a new block type can be defined for each usage	Yes
Block 0 Offset	0x6	2	Offset of block 0	Yes
Block 0 Length	0x8	2	Length of block 0 in bytes	Yes
Block 0 Reserved	0xA	2	Must be 0	Yes
Block 1 Type	0xC	2	See Block 0 type	Yes
Block 1 Offset	0xE	2	Offset of block 1	Yes
Block 1 Length	0x10	2	Length of block 1 in bytes	Yes
Block 1 Reserved	0x12	2	Must be 0	Yes



Name	Offset	Size (bytes)	Description	FIT Visible
.....				Yes
Block 'n' Type		2	See Block 0 type	Yes
Block 'n' Offset		2	Offset of block 'n'	Yes
Block 'n' Length		2	Length of block 'n' in bytes	Yes
Block 'n' Reserved		2	Must be 0	Yes

#### 4.1.7 Intel® ME Vendor Specific Component Capabilities Table

Entries in this table allow support for a SPI flash part for Intel Management Engine capabilities including Intel® Active Management Technology.

Since Flash Partition Boundary Address (FPBA) has been removed, UVSCC and LVSCC has been replaced with VSCC0 and VSCC1 in Cannonlake PCH-LP. VSCC0 is for SPI component 0 and VSCC1 is for SPI component 1.

Each VSCC table entry is composed of two 32 bit fields: JEDEC IDn and the corresponding VSCCn value.

See [4.4 Intel® ME Vendor-Specific Component Capabilities \(Intel® ME VSCC\) Table](#) for information on how to program individual entries.

##### 4.1.7.1 JID0—JEDEC-ID 0 Register (Flash Descriptor Records)

Memory Address: VTBA + 000h

Size: 32 bits

Bits	Description	FIT Visible
31:24	Reserved	No
23:16	<b>SPI Component Device ID 1.</b> This field identifies the second byte of the Device ID of the SPI Flash Component. This is the third byte returned by the Read JEDEC-ID command (opcode 9Fh).	Yes
15:8	<b>SPI Component Device ID 0.</b> This field identifies the first byte of the Device ID of the SPI Flash Component. This is the second byte returned by the Read JEDEC-ID command (opcode 9Fh).	Yes
7:0	<b>SPI Component Vendor ID.</b> This field identifies the one byte Vendor ID of the SPI Flash Component. This is the first byte returned by the Read JEDEC-ID command (opcode 9Fh).	Yes

##### 4.1.7.2 VSCC0—Vendor Specific Component Capabilities 0 (Flash Descriptor Records)

Memory Address: VTBA + 004h

Size: 32 bits

**Note:** VSCC0 applies to SPI flash that connected to CS0.

Bits	Description	FIT Visible
31:16	Reserved	No
15:8	<b>Erase Opcode (EO).</b> This field must be programmed with the Flash erase instruction opcode that corresponds to the erase size that is in BES.	No



Bits	Description	FIT Visible
7:5	<b>Quad Enable Requirements (QER)</b> 000 = Device does not have a QE bit. Device detects 1-1-4 and 1-4-4 reads based on instruction. DQ3 / HOLD# functions as hold during instruction phase. 001 = QE is bit 1 of status register 2. It is set via Write Status with two data bytes where bit 1 of the second byte is one. It is cleared via Write Status with two data bytes where bit 1 of the second byte is zero. Writing only one byte to the status register has the side effect of clearing status register 2, including the QE bit. The 100b code is used if writing one byte to the status register does not modify status register 2. 010 = QE is bit 6 of status register 1. It is set via Write Status with one data byte where bit 6 is one. It is cleared via Write Status with one data byte where bit 6 is zero. 011 = QE is bit 7 of status register 2. It is set via Write status register 2 instruction 3Eh with one data byte where bit 7 is one. It is cleared via Write status register 2 instruction 3Eh with one data byte where bit 7 is zero. The status register 2 is read using instruction 3Fh. 100 = QE is bit 1 of status register 2. It is set via Write Status with two data bytes where bit 1 of the second byte is one. It is cleared via Write Status with two data bytes where bit 1 of the second byte is zero. In contrast to the 001b code, writing one byte to the status register does not modify status register 2. 101 = QE is bit 1 of the status register 2. Status register 1 is read using Read Status instruction 05h. Status register 2 is read using instruction 35h. QE is set via Write Status instruction 01h with two data bytes where bit 1 of the second byte is one. It is cleared via Write Status with two data bytes where bit 1 of the second byte is zero. other = reserved <b>Note:</b> Please refer to Table note#1 below for details.	No
4:0	Reserved set to 00101b	No
<b>Notes:</b> 1. The manufacturers information included in the QER list are for guidance purpose. Some manufacturer devices operate as shown in the table above. Check manufacturer's data sheet for exact requirements.		

#### 4.1.7.3 JIDn—JEDEC-ID Register n (Flash Descriptor Records)

Memory Address: VTBA + (n\*8)h                      Size: 32 bits

"n" is an integer denoting the index of the Intel® ME VSCC table. See **Table 4.1.7.1** for details.

#### 4.1.7.4 VSCCn—Vendor Specific Component Capabilities n (Flash Descriptor Records)

Memory Address: VTBA + 0C4h + (n\*8)h                      Size: 32 bits

"n" is an integer denoting the index of the Intel® ME VSCC table. See **Table 4.1.7.2** for details.

## 4.2 OEM Section

Memory Address: F00h                      Size: 256 Bytes

256 Bytes are reserved at the top of the Flash Descriptor for use by the OEM. The information stored by the OEM can only be written during the manufacturing process as the Flash Descriptor read/write permissions must be set to Read Only when the computer leaves the manufacturing floor. The PCH Flash controller does not read this information. FFh is suggested to reduce programming time.



## 4.3 Region Access Control

Regions of the flash can be defined from read or write access by setting a protection parameter in the Master section of the Descriptor. There are only four masters that have the ability to access other regions: CPU/BIOS, Intel® ME Firmware, GbE software/driver running on CPU and EC.

Table 4-1. Region Access Control Table Options

Master Read/Write Access				
Region (#)	CPU / BIOS	IFWI (Intel® ME)	GbE Controller	EC
Descriptor (0)	Read Only	Read Only	Not Accessible	Not Accessible
BIOS (1)	CPU / BIOS can always read from and write to BIOS region prior to EOP	Not Accessible	Not Accessible	Not Accessible
IFWI / Intel® Management Engine (2)	Read / Write (BIOS Only)	Intel® ME can always read from and write to IFWI region	Not Accessible	Not Accessible
GbE (3)	Not Accessible	Read / Write	GbE software can always read from and write to GbE region	Not Accessible
PDR (4)	Not Accessible	Not Accessible	Not Accessible	Not Accessible
EC - Embedded Controller (Optional) (8)	Read / Write	Not Accessible	Not Accessible	EC can always read from and write to EC region
<b>Notes:</b> <ol style="list-style-type: none"> <li>1. The Region Access values listed above represent post manufacturing configuration only.</li> <li>2. Descriptor and PDR region is not a master, so they will not have Master R/W access.</li> <li>3. Descriptor should NOT have write access by any master in production systems.</li> <li>4. PDR region should only have read and/or write access by CPU/Host. GbE and ME should NOT have access to PDR region.</li> </ol>				





### 4.3.1 Intel Recommended Permissions for Region Access

The following Intel recommended read/write permissions are necessary to secure Intel® ME and Intel® ME FW.

**Table 4-2. Recommended Read/Write Permissions**

Master Access	Descriptor Region Bit 0	BIOS Region Bit1	IFWI / Intel® ME Region Bit2	GbE Region Bit3	PDR Region Bit4	EC Region Bit8
ME read access	Y	N	Y	Y	N	N
ME write access	N	N	Y	N	N	N
GbE read access	Y	N	N	Y	N	N
GbE write access	N	N	N	Y	N	N
BIOS read access	Y	Y	Y	Y	‡	†
BIOS write access	N	Y	N	Y	‡	†
EC read access	Y	*	N	N	N	Y
EC write access	N	N	N	N	N	Y
<b>Note:</b> 1. ‡ = Host access to PDR is the discretion of the customer. Implementation of PDR is optional. 2. † = Optional BIOS access to the EC region. 3. * = Optional EC Read access to BIOS.						

The table below shows the values to be inserted into the Flash image tool. The values below will provide the access levels described in the table above.

**Warning:** Pre-configuring the flash image to Intel recommended read / write permission through the Intel® FIT tool and then flashing the resulting image will cause the platform to enter into end-of-manufacturing flow which will result in the FPFs being permanently set in the PCH if the HW binding has been enabled in the Intel® FIT tool, or if the platform is using a revenue PCH/MCP.

**Table 4-3. Recommended Read/Write Settings for Platforms**

	ME	GbE	BIOS	EC
Read	0b 0000 0000 0000 1101 = 0x000D	0b 0000 0000 0000 1001 = 0x0009	0b 0000 000† 000‡ 1111 = 0x0†‡F	0b 0000 0001 0000 00*1 = 0x0101 or 0x0103
Write	0b 0000 0000 0000 0100 = 0x0004	0b 0000 0000 0000 1000 = 0x0008	0b 0000 000† 000‡ 1010 = 0x0†‡A	0b 0000 0001 0000 0000 = 0x0100
<b>Note:</b> 1. ‡ = Value dependent on if PDR is implemented and if Host access is desired. 2. † = Optional BIOS access to the EC region. 3. * = Optional EC Read access to BIOS.				

### 4.3.2 Overriding Region Access

Once access Intel recommended Flash settings have been put into the flash descriptor, it may be necessary to update the ME region with a Host program or write a new Flash descriptor.

Assert HDA\_SDO HIGH during the rising edge of PWROK to set the Flash descriptor override strap.

This strap should only be visible and available in manufacturing or during product development.

After this strap has been set you can use a host based flash programming tool like FPT to write/read any area of serial flash that is not protected by Protected Range Registers. Any area of flash protected by Protected range Registers will still NOT be writeable/readable.

See [6.3 SPI Protected Range Register Recommendations](#) for more details.



## 4.4 Intel® ME Vendor-Specific Component Capabilities (Intel® ME VSCC) Table

The Intel® ME VSCC Table defines how the Intel® ME will communicate with the installed SPI flash if there is no SFDP table found. This table is defined in the descriptor and is the responsibility of who puts together the NVM image. VSCCn registers are defined in memory space and must be set by BIOS. This table must define every flash part that is intended to be used. The size (number of max entries) of the table is defined in [4.1.6.1 FLUMAP1—Flash Upper Map 1 \(Flash Descriptor Records\)](#). Each Table entry is made of two parts: the JEDEC ID and VSCC setting.

Table 4-4. Jidn - JEDEC ID Portion of Intel® ME VSCC Table

Bits	Description	FIT Visible
31:24	Reserved.	No
23:16	<b>SPI Component Device ID 1:</b> This identifies the second byte of the Device ID of the SPI Flash Component. This is the third byte returned by the Read JEDEC-ID command (opcode 9Fh).	Yes
15:8	<b>SPI Component Device ID 0:</b> This identifies the first byte of the Device ID of the SPI Flash Component. This is the second byte returned by the Read JEDEC-ID command (opcode 9Fh).	Yes
7:0	<b>SPI Component Vendor ID:</b> This identifies the one byte Vendor ID of the SPI Flash Component. This is the first byte returned by the Read JEDEC-ID command (opcode 9Fh).	Yes

If using Flash Image Tool (FIT) refer to System Tools user guide in the Intel® ME FW kit and the respective FW Bring up Guide on how to build the image. If not, refer to [4.1.6.1 FLUMAP1—Flash Upper Map 1 \(Flash Descriptor Records\)](#) thru [4.2 OEM Section](#).

### 4.4.1 How to Set a VSCC Entry in Intel® ME VSCC Table for Cannonlake PCH-LP Platforms

VSCC0 needs to be programmed in instances where there is only SPI component in the system. When using an asymmetric flash component (part with two different sets of attributes based on address) VSCC0 and VSCC1 will need to be used. This includes if the system is intended to support both symmetric AND asymmetric SPI flash parts.

Refer to [4.4.2 Intel® ME VSCC Table Settings for Cannonlake PCH-LP Family Systems](#).

See text below the table for explanation on how to determine Intel Management Engine VSCC value.

Table 4-5. Vscn – Vendor-Specific Component Capabilities Portion of the Cannonlake PCH-LP Platforms (Sheet 1 of 2)

Bits	Description	FIT Visible
31:16	Reserved	
15:8	<b>Erase Opcode (EO).</b> This field must be programmed with the Flash erase instruction opcode that corresponds to the erase size that is in BES.	



**Table 4-5. Vscn – Vendor-Specific Component Capabilities Portion of the Cannonlake PCH-LP Platforms (Sheet 2 of 2)**

Bits	Description	FIT Visible
7:5	<b>Quad Enable Requirements (QER)</b> 000 = Part does not require a Quad Enable bit to be set, either because Quad is not supported or because the manufacturer permanently enables Quad capability (e.g. Micron, Numonyx). 001 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to status register clears all bits in register 2, therefore status register writes MUST be two bytes. If the status register is unlocked and SFDP bits WSR or VSCC WSR is 1 then SPI controller cannot use the quad output, quad IO features of this part because the hardware will automatically write one byte of zeros to status register with every write/erase. (e.g. Winbond, AMIC, Spansion). 010 = Part requires bit 6 of status register 1 to be set to enable quad IO. If the status register is unlocked and SFDP WSR bit or VSCC WSR is 1 then flash controller cannot use the quad output, quad IO features of this part because the hardware will automatically write one byte of zeros to status register with every write/erase (e.g. Macronix). 011 = Part requires bit 7 of the configuration register to be set to enable Quad (e.g. Atmel). 100 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to the status register does not clear the second byte (SST/Microchip, Winbond).  <b>Note:</b> Please refer to Table note#6 below for details.	No
4	<b>Write Enable on Write Status (WEWS)</b> 0 = 50h is the opcode used to unlock the status register on SPI flash if <b>WSR</b> (bit 3) is set to 1b. 1 = 06h is the opcode used to unlock the status register on SPI flash if <b>WSR</b> (bit 3) is set to 1b. <b>Note:</b> Please refer to Table Note #4 below for a description how this bit is used.	No
3	<b>Write Status Required (WSR)</b> 0 = No automatic write of 00h will be made to the SPI flash's status register) 1 = A write of 00h to the SPI flash's status register will be sent on EVERY write and erase performed by Intel® ME to the SPI flash. <b>Note:</b> Please refer to Table Note #5 below for a description how this bit is used.	No
2	<b>Write Granularity (WG).</b> 0 = 1 Byte 1 = 64 Bytes	No
1:0	<b>Block/Sector Erase Size (BES).</b> This field identifies the erasable sector size for all Flash components. 00 = 256 Bytes 01 = 4 K Bytes 10 = 8 K Bytes 11 = 64K Bytes	No
<b>Notes:</b> 1. Bit 3 ( <b>WEWS</b> ) and/or bit 4 ( <b>WSR</b> ) should not be set to '1' if there are non volatile bits in the SPI flash's status register. This may lead to premature flash wear out. 2. This is not an atomic (uninterrupted) sequence. The PCH will not wait for the status write to complete before issuing the next command, potentially causing SPI flash instructions to be disregarded by the SPI flash part. If the SPI flash component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. 3. If both bits 3 ( <b>WSR</b> ) and 4 ( <b>WEWS</b> ) are set to 1b, then sequence of 06h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs. 4. If bit 3 ( <b>WSR</b> ) is set to 1b and bit 4 ( <b>WEWS</b> ) is set to 0b then sequence of 50h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs. 5. If bit 3 ( <b>WSR</b> ) is set to 0b and bit 4 ( <b>WEWS</b> ) is set to 0b or 1b then sequence of 60h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs. 6. The manufacturers information included in the QER list are for guidance purpose. Some manufacturer devices operate as shown in the table above. Check manufacturer's datasheet for exact requirements.		

**Erase Opcode (EO) and Block/Sector Erase Size (BSES)** should be set based on the flash part and the firmware on the platform. For Intel® ME enabled platforms this should be 4 KB.

**Write Status Required (WSR) or Write Enable on Write Status (WEWS)** should be set on flash devices that require an opcode to enable a write to the status register. Intel® ME Firmware will write a 00h to status register to unlock the flash part for every erase/write operation. If this bit is set on a flash part that has non-volatile bits in the status register then it may lead to pre-mature wear out of the flash.



- Set the **WSR** bit to 1b and **WEWS** to 0b if the Enable Write Status Register opcode (50h) is needed to unlock the status register. Opcodes sequence sent to SPI flash will be 50h 01h 00h.
- Set the **WSR** bit to 1b AND **WEWS** bit to 1b if write enable (06h) will unlock the status register. Opcodes sequence sent to SPI flash will be 06h 01h 00h.
- Set the **WSR** bit to 0b AND **WEWS** bit to 0b or 1b, if write enable (06h) will unlock the status register. Opcodes sequence sent to SPI flash will be 06h
- **WSR or WEWS should be not be set on devices that use non volatile memory for their status register.** Setting this bit will cause operations to be ignored, which may cause undesired operation. Ask target flash vendor if this is the case for the target flash. See [6.1 Unlocking SPI Flash Device Protection for Cannonlake PCH-LP Platform](#) and [6.2 Locking SPI Flash via Status Register](#) for more information.

**Erase Opcode (EO)** and **Block/Sector Erase Size (BES)** should be set based on the flash part and the firmware on the platform.

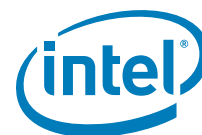
**Write Granularity (WG)** bit should be set based on the capabilities of the flash device. If the flash part is capable of writing 1 to 64 bytes (or more) with the 02h command you can set this bit 0 or 1. Setting this bit high will result in faster write performance. If flash part only supports single byte write only, then set this bit to 0.

**Bit ranges 31:16 and 7:5** are reserved and should be set to all zeros.

#### 4.4.2 Intel® ME VSCC Table Settings for Cannonlake PCH-LP Family Systems

To understand general guidelines for BIOS VSCC settings on different SPI flash devices, please refer to **VSCCommn.bin Content application note** (VSCCommn\_bin Content.pdf under Flash Image Tool directory).

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## 5 Serial Flash Discoverable Parameter (SFDP) Overview

### 5.1 Introduction

As the feature set of serial flash progresses, there is an increasing amount of divergence as individual vendors find different solution to adding new functionality such as speed and addressing.

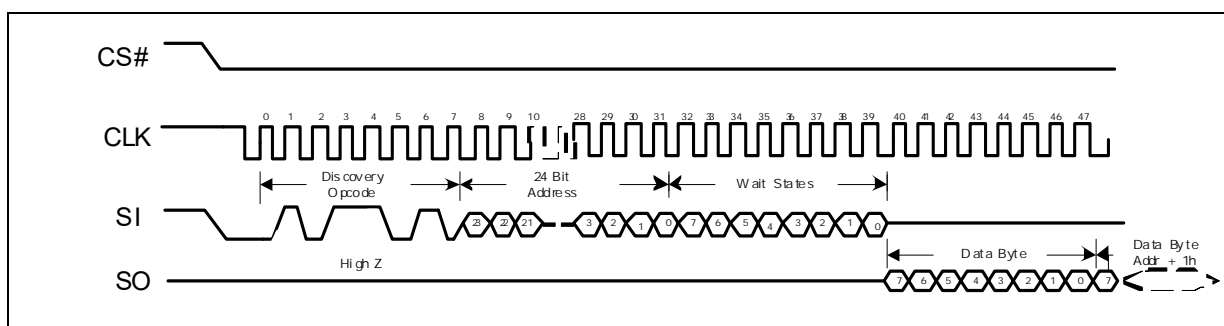
These guidelines are a standard that will allow for individual vendors to have their value add features, but will allow for a controller to discover the attributes needed to operate.

### 5.2 Discoverable Parameter Opcode and Flash Cycle

The discoverable parameter read opcode behaves like a fast read command. The opcode is 5Ah and the address cycle is 24 bit long. After the opcode 5Ah is clocked in, there are 24 bit of address clocked in. There will then be eight clock (8 wait states) before valid data is clocked out. There is flexibility in the number of wait states, but they must be byte aligned (multiple of 8 wait states).

SFDP read must update at a frequency between 17 MHz and 48 MHz with a single byte of wait state.

Figure 5-1. SFDP Read Instruction Sequence



### 5.3 Parameter Table Supported on PCH

The flash controller first checks for a valid SFDP header. The value of the major and minor revision fields in the SFDP header are don't care. If a valid SFDP header is found, the controller supports auto discovery of the Component Property Parameter Table (CPPT).

The following capabilities are only supported on PCH if CPPT is successfully discovered and parameter values indicate that they are supported. These capabilities are not supported as default.

- Quad I/O Read
- Quad Output Read



- Dual I/O read
- Dual Output Read
- Block /Sector Erase size

**Note:** If SFDP is valid and advertises 4 Kbyte erase capability, then BES is taken from the SFDP table, otherwise it is taken from the BIOS VCSS table.

PCH will also read the following opcode from parameter table and store to PCH if SFDP is valid and the following function is supported.

- Erase Opcode
- Dual Output Fast Read Opcode
- Dual I/O Fast Read Opcode
- Quad Output Fast Read Opcode
- Quad I/O Fast Read Opcode

## 5.4 Detailed JEDEC Specification

Please refer to [www.jedec.com](http://www.jedec.com) JESD216 for detailed SFDP specification on SPI.

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## 6 Configuring BIOS/GbE for SPI Flash Access

### 6.1 Unlocking SPI Flash Device Protection for Cannonlake PCH-LP Platform

BIOS must account for any built in protection from the flash device itself. BIOS must ensure that any flash based protection will only apply to BIOS region only. It should not affect the ME or GbE regions.

All the SPI flash devices that meet the SPI flash requirements in the *Cannonlake PCH-LP Family External Design Specification (EDS)* will be unlocked by writing a 00h to the SPI flash's status register. This command must be done via an atomic software sequencing to account for differences in flash architecture. Atomic cycles are uninterrupted in that it does not allow other commands to execute until a read status command returns a 'not busy' result from the flash.

Some flash vendors implement their status registers in NVM flash (non-volatile memory). This takes much more time than a write to volatile memory. During this write, the flash part will ignore all commands but a read to the status register (opcode 05h). The output of the read status register command will tell the PCH when the transaction is done.

Recommended flash unlocking sequence:

- Write enable (06h) command will have to be in the prefix opcode configuration register.
- The "write to status register" opcode (01h) will need to be an opcode menu configuration option.
- Opcode type for write to status register will be '01': a write cycle type with no address needed.
- The FDATA0 register should to be programmed to 0000 0000h.
- Data Byte Count (DBC) in Software Sequencing Flash Control register should be 000000b. Errors may occur if any non zero value is here.
- Set the Cycle Opcode Pointer (COP) to the "write to status register" opcode.
- Set to Sequence Prefix Opcode Pointer (SPOP) to Write Enable.
- Set the Data Cycle (DS) to 1.
- Set the Atomic Cycle Sequence (ACS) bit to 1.
- To execute sequence, set the SPI Cycle Go bit to 1.

Please see the ***Serial Peripheral Interface Memory Mapped Configuration Registers*** in the *Cannonlake PCH-LP Family External Design Specification (EDS)* for more detailed information.



## 6.2 Locking SPI Flash via Status Register

Flash vendors that implement their status register with non-volatile memory can be updated a limited number of times. This means that this register may wear out before the desired endurance for the rest of the flash. It is highly recommended that BIOS vendors and customers do NOT use the SPI flash's status register to protect the flash in multiple master systems.

BIOS should try to minimize the number of times that the system is locked and unlocked.

Care should be taken when using status register based SPI flash protection in multiple master systems such as Intel® ME FW and/or integrated GbE. BIOS must ensure that any flash based protection will apply to BIOS region only. It should not affect the ME or GbE regions.

Please contact your desired flash vendor to see if their status register protection bits volatile or non-volatile. Flash parts implemented with volatile systems do not have this concern.

## 6.3 SPI Protected Range Register Recommendations

The PCH has a mechanism to set up to 5 address ranges from HOST access. These are defined in PR0, PR1, PR2, PR3 and PR4 in the PCH EDS. These address ranges are NOT unlocked by assertion of Flash descriptor Override.

It is strongly recommended to use a protected range register to lock down the factory default portion of Intel® ME FW region. The runtime portion should be left unprotected as to allow BIOS to update it.

It is strongly recommended that if Flash Descriptor Override strap (which can be checked by reading **FDOPSS (0b Flash Descriptor override is set, 1b not set) in PCH memory space (SPIBAR+C4h bit 13))** is set, do not set a Protected range to cover the Intel® ME FW factory defaults. This would allow a flashing of a complete image when the Flash descriptor Override strap is set.

## 6.4 Recommendations for Flash Configuration Lockdown and Vendor Component Lock Bits

### 6.4.1 Flash Configuration Lockdown

It is strongly recommended that BIOS sets the Host and GbE **Flash Configuration Lock-Down (FLOCKDN)** bits (located at SPIBAR + 04h and MBAR +04h respectively) to '1' on production platforms. If these bits are not set, it is possible to make register changes that can cause undesired host, integrated GbE and Intel® ME functionality as well as lead to unauthorized flash region access.

Refer to **HSFS— Hardware Sequencing Flash Status Register** in the Serial Peripheral Interface Memory Mapped Configuration Registers section and **HSFS— Hardware Sequencing Flash Status Register** in the GbE SPI Flash Programming Registers section in the Cannonlake PCH-LP Family External Design Specification (EDS).





## 6.4.2 Vendor Component Lock

It is strongly recommended that BIOS sets the **Vendor Component Lock (VCL)** bits. These bits are located in the BIOS/GbE VSCC0 registers. VCL applies the lock to both VSCC0 and VSCC1 even if VSCC1 is not used. Without the VCL bits set, it is possible to make Host/GbE VSCC register(s) changes in that can cause undesired host and integrated GbE SPI flash functionality.

Refer to **VSCC— Vendor Specific Component Capabilities Register** in the Cannonlake *PCH-LP Family External Design Specification (EDS)* for more information.

## 6.5 Host Vendor Specific Component Control Registers (VSCC)

VSCC are memory mapped registers are used by the PCH when BIOS or Integrate LAN reads, programs or erases the SPI flash via Hardware sequencing.

Flash Partition Boundary Address (FBPBA) has been removed and UVSCC and LVSCC has been replaced with VSCC0 and VSCC1 in Cannonlake PCH-LP. VSCC0 is for SPI component 0 and VSCC1 is for SPI component 1. SPI controller will determine which VSCC (VSCC0 or VSCC1) to be used by comparing Flash Linear Address (FLA) with size of SPI component 0 (CODEN). When  $FLA \leq CODEN$  then VSCC0 will be used; whereas  $FLA > CODEN$  then VSCC1 will be used. If one SPI flash component used in the system, VSCC0 needs to be set.

Refer to **VSCC— Lower Vendor Specific Component Capabilities Register** and in the *Cannonlake PCH-LP Family External Design Specification (EDS)*.

See text below the tables for explanation on how to determine VSCC register values.

**Table 6-1. VSCC0 - Vendor-Specific Component Capabilities Register for SPI Component 0 (Sheet 1 of 3)**

Bit	Description
31	<b>Component Property Parameter Table Valid (CPPTV) - RO:</b> This bit is set to a 1 if the Flash Controller detects a valid SFDP Component Property Parameter Table in SPI Component 0 If CPPTV bit is '0', software must configure the VSCC register appropriately. If CPPTV bit is '1', the corresponding parameter values discovered via SFDP will be used. In most cases, software is not required to configure the VSCC register. However, if the SFDP table indicates an erase size other than 4k byte, then the software is required to program the VSCC.EO register with the correct erase opcode.
30:24	Reserved
23	<b>Vendor Component Lock (VCL): — RW/L:</b> '0': The lock bit is not set '1': The Vendor Component Lock bit is set.  This register locks itself when set.  This bit applies to both VSCC0 and VSCC1 All bits locked by (VCL) will remained locked until a global reset.
22:16	Reserved



**Table 6-1. VSCC0 - Vendor-Specific Component Capabilities Register for SPI Component 0 (Sheet 2 of 3)**

Bit	Description
15:8	<p><b>Erase Opcode (EO)</b>— RW:</p> <p>This register is programmed with the Flash erase instruction opcode required by the vendor's Flash component. Software must program this register if the SFDP table for this component does not show 4 kByte erase capability</p> <p>This register is locked by the Vendor Component Lock (VCL) bit.</p> <p><b>Note:</b> If CPPTV is 1 and the SPDP0 table shows 4k erase capability, the SFDP0 erase code is used instead of this register</p>
7:5	<p><b>Quad Enable Requirements (QER)</b></p> <p>000 = Part does not require a Quad Enable bit to be set, either because Quad is not supported or because the manufacturer permanently enables Quad capability (e.g. Micron, Numonyx).</p> <p>001 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to status register clears all bits in register 2, therefore status register writes MUST be two bytes. If the status register is unlocked and SFDP bits WSR or VSCC WSR is 1 then SPI controller cannot use the quad output, quad IO features of this part because the hardware will automatically write one byte of zeros to status register with every write/erase. (e.g. Winbond, AMIC, Spansion).</p> <p>010 = Part requires bit 6 of status register 1 to be set to enable quad IO. If the status register is unlocked and SFDP WSR bit or VSCC WSR is 1 then flash controller cannot use the quad output, quad IO features of this part because the hardware will automatically write one byte of zeros to status register with every write/erase (e.g. Macronix).</p> <p>011 = Part requires bit 7 of the configuration register to be set to enable Quad (e.g. Atmel).</p> <p>100 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to the status register does not clear the second byte (SST/Microchip, Winbond).</p> <p><b>Note:</b> This register is locked by the Vendor Component Lock (VCL) bit.</p>
4	<p><b>Write Enable on Write Status (WEWS)</b> — RW:</p> <p>'0' = 50h will be the opcode used to unlock the status register on the SPI flash if <b>WSR</b> (bit 3) is set to 1b.</p> <p>'1' = 06h will be the opcode used to unlock the status register on the SPI flash if <b>WSR</b> (bit 3) is set to 1b.</p> <p>This register is locked by the Vendor Component Lock (VCL) bit.</p> <p><b>Note:</b> Please refer to <a href="#">Table 6-3</a> for a description of how these bits is used.</p>
3	<p><b>Write Status Required (WSR)</b> — RW:</p> <p>'0' = No automatic write of 00h will be made to the SPI flash's status register.</p> <p>'1' = A write of 00h to the SPI flash's status register will be sent on EVERY write and erase to the SPI flash performed by Host and GbE.</p> <p>This register is locked by the Vendor Component Lock (VCL) bit.</p> <p><b>Note:</b> Please refer to <a href="#">Table 6-3</a> for a description of how these bits is used.</p>
2	<p><b>Write Granularity (WG)</b> — RW:</p> <p>0: 1 Byte</p> <p>1: 64 Byte</p> <p>This register is locked by the Vendor Component Lock (VCL) bit.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>If more than one Flash component exists, this field must be set to the lowest common write granularity of the different Flash components</li> <li>If using 64 B write, BIOS must ensure that multiple byte writes do not occur over 256 B boundaries. This will lead to corruption as the write will wrap around the page boundary on the SPI flash part. This is a feature in page writable SPI flash.</li> </ol>



**Table 6-1. VSCC0 - Vendor-Specific Component Capabilities Register for SPI Component 0 (Sheet 3 of 3)**

Bit	Description
1:0	<p><b>Block/Sector Erase Size (BES)— RW:</b>  This field identifies the erasable sector size for Flash components.  Valid Bit Settings:  00: 256 Byte  01: 4 KByte  10: 8 KByte  11: 64 K  This register is locked by the Vendor Component Lock (VCL) bit.  Hardware takes no action based on the value of this register. The contents of this register are to be used only by software and can be read in the HSFSTS.BERASE register in both the BIOS and the GbE program registers if FLA is less than FPBA.</p>

**Table 6-2. VSCC1 - Vendor Specific Component Capabilities Register for SPI Component 1 (Sheet 1 of 2)**

Bit	Description
31	<p><b>Component Property Parameter Table Valid (CPPTV) - RO:</b>  This bit is set to a 1 if the Flash Controller detects a valid SFDP Component Property Parameter Table in SPI Component 1  If CPPTV bit is '0', software must configure the VSCC register appropriately. If CPPTV bit is '1', the corresponding parameter values discovered via SFDP will be used. In most cases, software is not required to configure the VSCC register. However, if the SFDP table indicates an erase size other than 4k byte, then the software is required to program the VSCC.EO register with the correct erase opcode.</p>
30:16	Reserved
15:8	<p><b>Erase Opcode (EO)— RW:</b>  This register is programmed with the Flash erase instruction opcode required by the vendor's Flash component.  This register is locked by the Vendor Component Lock (VCL) bit.</p>
7:5	<p><b>Quad Enable Requirements (QER)</b>  000 = Part does not require a Quad Enable bit to be set, either because Quad is not supported or because the manufacturer permanently enables Quad capability (e.g. Micron, Numonyx).  001 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to status register clears all bits in register 2, therefore status register writes MUST be two bytes. If the status register is unlocked and SFDP WSR or VSCC WSR is 1 then SPI controller cannot use the quad output, quad IO features of this part because the hardware will automatically write one byte of zeros to status register with every write/erase. (e.g. Winbond, AMIC, Spansion).  010 = Part requires bit 6 of status register 1 to be set to enable quad IO. If the status register is unlocked and SFDP WSR bit or VSCC WSR is 1 then flash controller cannot use the quad output, quad IO features of this part because the hardware will automatically write one byte of zeros to status register with every write/erase (e.g. Macronix).  011 = Part requires bit 7 of the configuration register to be set to enable Quad (e.g. Atmel).  100 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to the status register does not clear the second byte (SST/Microchip, Winbond).  <b>Note:</b> This register is locked by the Vendor Component Lock (VCL) bit.</p>
4	<p><b>Write Enable on Write to Status (WEWS) — RW:</b>  '0' = 50h will be the opcode used to unlock the status register if <b>WSR</b> (bit 3) is set to 1b.  '1' = 06h will be the opcode used to unlock the status register if <b>WSR</b> (bit 3) is set to 1b.  This register is locked by the Vendor Component Lock (VCL) bit.  Please refer to <a href="#">Table 6-3</a> for a description of how these bits is used.</p>



**Table 6-2. VSCC1 - Vendor Specific Component Capabilities Register for SPI Component 1 (Sheet 2 of 2)**

Bit	Description
3	<p><b>Write Status Required (WSR)</b> — RW:</p> <p>'0' = No automatic write of 00h will be made to the SPI flash's status register</p> <p>'1' = A write of 00h to the SPI flash's status register will be sent on EVERY write and erase to the SPI flash performed by Host and GbE.</p> <p>This register is locked by the Vendor Component Lock (VCL) bit.</p> <p><b>Note:</b> Please refer to <a href="#">Table 6-3</a> for a description of how these bits is used.</p>
2	<p><b>Write Granularity (WG)</b> — RW:</p> <p>0: 1 Byte</p> <p>1: 64 Byte</p> <p>This register is locked by the Vendor Component Lock (VCL) bit.</p> <p>If more than one Flash component exists, this field must be set to the lowest common write granularity of the different Flash components.</p> <p>If using 64 B write, BIOS must ensure that multiple byte writes do not occur over 256 B boundaries. This will lead to corruption as the write will wrap around the page boundary on the SPI flash part. This is a feature in page writeable SPI flash.</p>
1:0	<p><b>Block/Sector Erase Size (BES)</b>— RW: This field identifies the erasable sector size for all Flash components.</p> <p>Valid Bit Settings:</p> <p>00: 256 Byte</p> <p>01: 4 KByte</p> <p>10: 8 KByte</p> <p>11: 64 K</p> <p>This register is locked by the Vendor Component Lock (VCL) bit.</p> <p>Hardware takes no action based on the value of this register. The contents of this register are to be used only by software and can be read in the HSFSTS.BERASE register in both the BIOS and the GbE program registers if FLA is less than FPBA.</p>

**Erase Opcode (EO)** and **Block/Sector Erase Size (BSES)** should be set based on the flash part and the firmware on the platform.

- Either **Write Status Required (WSR)** or **Write Enable on Write Status (WEWS)** should be set on flash devices that require an opcode to enable a write to the status register. BIOS and GbE will write a 00h to the SPI flash's status register to unlock the flash part for every erase/write operation. If this bit is set on a flash part that has non-volatile bits in the status register then it may lead to pre-mature wear out of the flash and may result in undesired flash operation. Please refer to [Table 6-3](#) for a description of how these bits is set and what is the expected operation from the controller during erase/write operation.

**Table 6-3. Description of How WSR and WEWS is Used**

WSR	WEWS	Flash Operation
1b	0b	If the Enable Write Status Register opcode (50h) is needed to unlock the status register. Opcodes sequence sent to SPI flash will bit 50h 01h 00h.
1b	1b	If write enable (06h) will unlock the status register. Opcodes sequence sent to SPI flash will bit 06h 01h 00h.
0b	0 or 1b	Sequence of 60h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs.



**Note:** **WSR or WEWS should be not be set on devices that use non volatile memory for their status register.** Setting this bit will cause operations to be ignored, which may cause undesired operation. Ask target flash vendor if this is the case for the target flash. See [6.1 Unlocking SPI Flash Device Protection for Cannonlake PCH-LP Platform](#) and [6.2 Locking SPI Flash via Status Register](#) for more information.

**Write Granularity (WG)** bit should be set based on the capabilities of the flash device. If the flash part is capable of writing 1 to 64 bytes (or more) with the 02h command you can set this bit 0 or 1. Setting this bit high will result in faster write performance. If flash part only supports single byte write only, then set this bit to 0. Setting this bit high requires that BIOS ensure that no multiple byte write operation does not cross a 256 Byte page boundary, as it will have unintended results. This is a feature of page programming capable flash parts.

**Vendor Component Lock (VCL)** should remain unlocked during development, but locked in shipping platforms. When **VCL** and **FLOCKDN** are set, it is possible that you may not be able to use in system programming methodologies including Intel Flash Programming Tool if programmed improperly. It will require a system reset to unlock this register and BIOS not to set this bits. See [6.4 Recommendations for Flash Configuration Lockdown and Vendor Component Lock Bits](#) for more details.

**All reserved bits** should set to zeros.

## 6.6 Host VSCC Register Settings

To understand general guidelines for VSCC settings with different SPI flash devices, please refer to **VSCCommn.bin content application note** (VSCCommn\_bin Content.pdf under Flash Image Tool directory). VSCCommn.bin contains SPI devices vendor ID, device ID and recommended VSCC values.

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# 7 IFWI / Intel® ME Disable for Debug/Flash Burning Purposes

This section is purely for debug purposes. Intel® ME FW is the only supported configuration for Cannonlake PCH-LP based system.

## 7.1 IFWI / Intel® ME Disable

Here are the ways one can disable the Intel® ME for purposes of in system programming the flash.

1. HDA\_SDO (Manufacturing mode jumper or Flash descriptor override jumper) asserted HIGH on the rising edge of PWROK. Power off or cold reset. Note: this is only valid as long as you do not specifically set the variable Flash Descriptor Override Pin-Strap Ignore in the Flash Image Tool to false.
2. HECI ME region unlock - There is a HECI command that allows Intel® ME FW to boot up in a temporarily disabled state and allows for a host program to overwrite the ME region.

**Note:** Removing the DIMM from channel 0 no longer has any effect on Intel® ME functionality.

### 7.1.1 Erasing/Programming Intel® ME Region

If CPU/Host has access to ME region, then one could either erase/program the ME region to all FFh. If there is no access, then one must assert HDA\_SDO (Flash descriptor override strap) HIGH during the rising edge of PWROK. If there are Protected Range registers set, then you will not be able to program this w/o a BIOS option to turn off this protected range. (See [6.3 SPI Protected Range Register Recommendations](#)) for more detail.

This depends on the board booting HW defaults for clock configuration. If any clock configuration is required for booting the platform that is not in the HW defaults, then this option may not work for you.

FPT will automatically disable SPI writing by the Intel ME when erasing any address in IFWI and ME Data regions.

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## 8 Recommendations for SPI Flash Programming in Manufacturing Environments

It is recommended that the Intel® ME be disabled when you are programming the ME region. Intel® ME FW performs regular writes/erases to the ME region. Therefore some bits may be changed after programming. Please note that not all of these options will be optimal for your manufacturing process.

**Any method of programming SPI flash where the system is not powered will not result in any interference from Intel® ME FW. The following methods are for Intel® ME FW:**

- Program via In Circuit Test – System is not fully powered here.
- Program via external flash burn-in solution.
- Assert HDA\_SDO HIGH (Flash Descriptor Override Jumper) on the rising edge of PWROK. Note: this is only valid as long as you do not specifically disable this functionality in fixed offset variable.

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## 9 Flash Descriptor PCH / PMC / CPU and Intel® ME Configuration Section

The following section describes functionality and how to set soft strapping for a target platform. Improper setting of soft straps can lead to undesired operation and may lead to returns/recalls.

### 9.1 PCH Descriptor Record 0 (Flash Descriptor Records)

Flash Address: FPSBA + 000h

Default Flash Address: 100h

Offset from 0	Bits	Description	Usage	FIT Visible
0x100h	7:0	Reserved, set to '0'		No

### 9.2 PCH Descriptor Record 1 (Flash Descriptor Records)

Flash Address: FPSBA + 001h

Default Flash Address: 101h

Offset from 0	Bits	Description	Usage	FIT Visible
0x101h	7:0	Reserved, set to '0'		No

### 9.3 PCH Descriptor Record 2 (Flash Descriptor Records)

Flash Address: FPSBA + 002h

Default Flash Address: 102h

Offset from 0	Bits	Description	Usage	FIT Visible
0x102h	7:0	Reserved, set to '0'		No

### 9.4 PCH Descriptor Record 3 (Flash Descriptor Records)

Flash Address: FPSBA + 003h

Default Flash Address: 103h

Offset from 0	Bits	Description	Usage	FIT Visible
0x103h	7:0	Reserved, set to '0'		No





## 9.5 PCH Descriptor Record 4 (Flash Descriptor Records)

Flash Address: FPSBA + 004h

Default Flash Address: 104h

Offset from 0	Bits	Description	Usage	FIT Visible
0x104h	7:6	Reserved, set to '0'		No
	5:4	<b>SATA / PCIe GP Select for Port 2 (SATA_PCIE_GP2):</b>  00 = PCIe Port 16 is statically assigned to SATA Port 2 01 = PCIe Port 16 is statically assigned to PCIe (or GbE) 10 = Reserved 11 = Assigned based on the polarity of SATAXPcie2 determined by SPS2	This strap must also be configured when setting the PCIe / SATA Combo Port 3 (PCIE_SATA_P3_Flex).  <b>Note:</b> This strap and the PCIe / SATA Combo Port 2 (PCIE_SATA_P3_Flex) and (SATA_PCIE_SP2) must match for proper port function.  <b>Note:</b> For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe*. These unused SATA/PCIe* Combo Lanes must not be assigned as polarity based.	No
	3:2	<b>SATA / PCIe GP Select for Port 1 (SATA_PCIE_GP1):</b>  00 = PCIe Port 12 or PCIe Port 15 is statically assigned to SATA Port 1 01 = PCIe Port 12 or PCIe Port 15 is statically assigned to PCIe (or GbE) 10 = Reserved 11 = Assigned based on the polarity of SATAXPcie1 determined by SPS1	This strap must also be configured when setting the PCIe / SATA Combo Port 1 Strap (PCIE_SATA_P1_Flex) or SATA / PCIe Combo Port 3 Strap (PCIE_SATA_P2_Flex).  <b>Note:</b> This strap and the PCIe / SATA Combo Port 1 Strap (PCIE_SATA_P1_Flex) or PCIe / SATA Combo Port 3 Strap (PCIE_SATA_P2_Flex) and (SATA_PCIE_SP1) must match for proper port function.  <b>Note:</b> For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe*. These unused SATA/PCIe* Combo Lanes must not be assigned as polarity based.	No
	1:0	<b>SATA / PCIe GP Select for Port 0 (SATA_PCIE_GPO):</b>  00 = PCIe Port 11 is statically assigned to SATA Port 0 01 = PCIe Port 11 is statically assigned to PCIe (or GbE) 10 = Reserved 11 = Assigned based on the polarity of SATAXPcie0 determined by SPS0	This strap must also be configured when setting the PCIe / SATA Combo Port 0 (PCIE_SATA_PO_Flex).  <b>Note:</b> This strap and the PCIe / SATA Combo Port 0 (PCIE_SATA_PO_Flex) and (SATA_PCIE_SPO) must match for proper port function.  <b>Note:</b> For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe*. These unused SATA/PCIe* Combo Lanes must not be assigned as polarity based.	No



## 9.6 PCH Descriptor Record 5 (Flash Descriptor Records)

Flash Address: FPSBA + 005h

Default Flash Address: 105h

Offset from 0	Bits	Description	Usage	FIT Visible
0x105h	7:3	Reserved, set to '0'		No
	2	<b>Intel® SMBus ASD Mode Configuration (SMBALERTB):</b>  0 = Configured as GPP_C2 1 = Configured as Intel® SMBus ASD	This setting determines the native mode for the SMBAlert signal.	Yes
	1:0	Reserved, set to '0'		No

## 9.7 PCH Descriptor Record 6 (Flash Descriptor Records)

Flash Address: FPSBA + 006h

Default Flash Address: 106h

Offset from 0	Bits	Description	Usage	FIT Visible
0x106h	7	<b>GPP_C7 Individual Voltage Select (GPPC_C7_VCCIO):</b>  0 = GPP_C7 Voltage set to 3.3v 1 = GPP_C7 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C7 GPIO pin.	Yes
	6	<b>GPP_C6 Individual Voltage Select (GPPC_C6_VCCIO):</b>  0 = GPP_C6 Voltage set to 3.3v 1 = GPP_C6 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C6 GPIO pin.	Yes
	5	<b>GPP_C5 Individual Voltage Select (GPPC_C5_VCCIO):</b>  0 = GPP_C5 Voltage set to 3.3v 1 = GPP_C5 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C5 GPIO pin.	Yes
	4	<b>GPP_C4 Individual Voltage Select (GPPC_C4_VCCIO):</b>  0 = GPP_C4 Voltage set to 3.3v 1 = GPP_C4 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C4 GPIO pin.	Yes
	3	<b>GPP_C3 Individual Voltage Select (GPPC_C3_VCCIO):</b>  0 = GPP_C3 Voltage set to 3.3v 1 = GPP_C3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C3 GPIO pin.	Yes
	2	<b>GPP_C2 Individual Voltage Select (GPPC_C2_VCCIO):</b>  0 = GPP_C2 Voltage set to 3.3v 1 = GPP_C2 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C2 GPIO pin.	Yes



Offset from 0	Bits	Description	Usage	FIT Visible
0x106h (Cont)	1	<b>GPP_C1 Individual Voltage Select (GPPC_C1_VCCIO):</b>  0 = GPP_C1 Voltage set to 3.3v 1 = GPP_C1 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C1 GPIO pin.	Yes
	0	<b>GPP_C0 Individual Voltage Select (GPPC_C0_VCCIO):</b>  0 = GPP_C0 Voltage set to 3.3v 1 = GPP_C0 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C0 GPIO pin.	Yes

## 9.8 PCH Descriptor Record 7 (Flash Descriptor Records)

Flash Address: FPSBA + 007h

Default Flash Address: 107h

Offset from 0	Bits	Description	Usage	FIT Visible
0x107h	7	<b>GPP_C15 Individual Voltage Select (GPPC_C15_VCCIO):</b>  0 = GPP_C15 Voltage set to 3.3v 1 = GPP_C15 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C15 GPIO pin.	Yes
	6	<b>GPP_C14 Individual Voltage Select (GPPC_C14_VCCIO):</b>  0 = GPP_C14 Voltage set to 3.3v 1 = GPP_C14 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C14 GPIO pin.	Yes
	5	<b>GPP_C13 Individual Voltage Select (GPPC_C13_VCCIO):</b>  0 = GPP_C13 Voltage set to 3.3v 1 = GPP_C13 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C13 GPIO pin.	Yes
	4	<b>GPP_C12 Individual Voltage Select (GPPC_C12_VCCIO):</b>  0 = GPP_C12 Voltage set to 3.3v 1 = GPP_C12 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C12 GPIO pin.	Yes
	3	<b>GPP_C11 Individual Voltage Select (GPPC_C11_VCCIO):</b>  0 = GPP_C11 Voltage set to 3.3v 1 = GPP_C11 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C11 GPIO pin.	Yes
	2	<b>GPP_C10 Individual Voltage Select (GPPC_C10_VCCIO):</b>  0 = GPP_C10 Voltage set to 3.3v 1 = GPP_C10 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C10 GPIO pin.	Yes
	1	<b>GPP_C9 Individual Voltage Select (GPPC_C9_VCCIO):</b>  0 = GPP_C9 Voltage set to 3.3v 1 = GPP_C9 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C9 GPIO pin.	Yes



Offset from 0	Bits	Description	Usage	FIT Visible
0x107h (Cont)	0	<b>GPP_C8 Individual Voltage Select (GPPC_C8_VCCIO):</b>  0 = GPP_C8 Voltage set to 3.3v 1 = GPP_C8 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C8 GPIO pin.	Yes

## 9.9 PCH Descriptor Record 8 (Flash Descriptor Records)

Flash Address: FPSBA + 008h

Default Flash Address: 108h

Offset from 0	Bits	Description	Usage	FIT Visible
0x108h	7	<b>GPP_C23 Individual Voltage Select (GPPC_C23_VCCIO):</b>  0 = GPP_C23 Voltage set to 3.3v 1 = GPP_C23 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C23 GPIO pin.	Yes
	6	<b>GPP_C22 Individual Voltage Select (GPPC_C22_VCCIO):</b>  0 = GPP_C22 Voltage set to 3.3v 1 = GPP_C22 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C22 GPIO pin.	Yes
	5	<b>GPP_C21 Individual Voltage Select (GPPC_C21_VCCIO):</b>  0 = GPP_C21 Voltage set to 3.3v 1 = GPP_C21 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C21 GPIO pin.	Yes
	4	<b>GPP_C20 Individual Voltage Select (GPPC_C20_VCCIO):</b>  0 = GPP_C20 Voltage set to 3.3v 1 = GPP_C20 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C20 GPIO pin.	Yes
	3	<b>GPP_C19 Individual Voltage Select (GPPC_C19_VCCIO):</b>  0 = GPP_C16 Voltage set to 3.3v 1 = GPP_C16 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C19 GPIO pin.	Yes
	2	<b>GPP_C18 Individual Voltage Select (GPPC_C18_VCCIO):</b>  0 = GPP_C16 Voltage set to 3.3v 1 = GPP_C16 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C18 GPIO pin.	Yes
	1	<b>GPP_C17 Individual Voltage Select (GPPC_C17_VCCIO):</b>  0 = GPP_C16 Voltage set to 3.3v 1 = GPP_C16 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C17 GPIO pin.	Yes
	0	<b>GPP_C16 Individual Voltage Select (GPPC_C16_VCCIO):</b>  0 = GPP_C16 Voltage set to 3.3v 1 = GPP_C16 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_C16 GPIO pin.	Yes



## 9.10 PCH Descriptor Record 9 (Flash Descriptor Records)

Flash Address: FPSBA + 009h

Default Flash Address: 109h

Offset from 0	Bits	Description	Usage	FIT Visible
0x109h	7	<b>GPP_E7 Individual Voltage Select (GPPC_E7_VCCIO):</b>  0 = GPP_C16 Voltage set to 3.3v 1 = GPP_C16 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E7 GPIO pin.	Yes
	6	<b>GPP_E6 Individual Voltage Select (GPPC_E6_VCCIO):</b>  0 = GPP_E6 Voltage set to 3.3v 1 = GPP_E6 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E6 GPIO pin.	Yes
	5	<b>GPP_E5 Individual Voltage Select (GPPC_E5_VCCIO):</b>  0 = GPP_E5 Voltage set to 3.3v 1 = GPP_E5 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E5 GPIO pin.	Yes
	4	<b>GPP_E4 Individual Voltage Select (GPPC_E4_VCCIO):</b>  0 = GPP_E4 Voltage set to 3.3v 1 = GPP_E4 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E4 GPIO pin.	Yes
	3	<b>GPP_E3 Individual Voltage Select (GPPC_E3_VCCIO):</b>  0 = GPP_E3 Voltage set to 3.3v 1 = GPP_E3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E3 GPIO pin.	Yes
	2	<b>GPP_E2 Individual Voltage Select (GPPC_E2_VCCIO):</b>  0 = GPP_E2 Voltage set to 3.3v 1 = GPP_E2 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E2 GPIO pin.	Yes
	1	<b>GPP_E1 Individual Voltage Select (GPPC_E1_VCCIO):</b>  0 = GPP_E1 Voltage set to 3.3v 1 = GPP_E1 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E1 GPIO pin.	Yes
	0	<b>GPP_E0 Individual Voltage Select (GPPC_E0_VCCIO):</b>  0 = GPP_E0 Voltage set to 3.3v 1 = GPP_E0 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E0 GPIO pin.	Yes



## 9.11 PCH Descriptor Record 10 (Flash Descriptor Records)

Flash Address: FPSBA + 00Ah

Default Flash Address: 10Ah

Offset from 0	Bits	Description	Usage	FIT Visible
0x10Ah	7	<b>GPP_E15 Individual Voltage Select (GPPC_E15_VCCIO):</b>  0 = GPP_E15 Voltage set to 3.3v 1 = GPP_E15 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E15 GPIO pin.	Yes
	6	<b>GPP_E14 Individual Voltage Select (GPPC_E14_VCCIO):</b>  0 = GPP_E14 Voltage set to 3.3v 1 = GPP_E14 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E14 GPIO pin.	Yes
	5	<b>GPP_E13 Individual Voltage Select (GPPC_E13_VCCIO):</b>  0 = GPP_E13 Voltage set to 3.3v 1 = GPP_E13 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E13 GPIO pin.	Yes
	4	<b>GPP_E12 Individual Voltage Select (GPPC_E12_VCCIO):</b>  0 = GPP_E12 Voltage set to 3.3v 1 = GPP_E12 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E12 GPIO pin.	Yes
	3	<b>GPP_E11 Individual Voltage Select (GPPC_E11_VCCIO):</b>  0 = GPP_E11 Voltage set to 3.3v 1 = GPP_E11 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E11 GPIO pin.	Yes
	2	<b>GPP_E10 Individual Voltage Select (GPPC_E10_VCCIO):</b>  0 = GPP_E10 Voltage set to 3.3v 1 = GPP_E10 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E10 GPIO pin.	Yes
	1	<b>GPP_E9 Individual Voltage Select (GPPC_E9_VCCIO):</b>  0 = GPP_E9 Voltage set to 3.3v 1 = GPP_E9 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E9 GPIO pin.	Yes
	0	<b>GPP_E8 Individual Voltage Select (GPPC_E8_VCCIO):</b>  0 = GPP_E8 Voltage set to 3.3v 1 = GPP_E8 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E8 GPIO pin.	Yes



## 9.12 PCH Descriptor Record 11 (Flash Descriptor Records)

Flash Address: FPSBA + 00Bh

Default Flash Address: 10Bh

Offset from 0	Bits	Description	Usage	FIT Visible
0x10Bh	7	<b>GPP_E23 Individual Voltage Select (GPPC_E23_VCCIO):</b>  0 = GPP_E23 Voltage set to 3.3v 1 = GPP_E23 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E23 GPIO pin.	Yes
	6	<b>GPP_E22 Individual Voltage Select (GPPC_E22_VCCIO):</b>  0 = GPP_E22 Voltage set to 3.3v 1 = GPP_E22 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E22 GPIO pin.	Yes
	5	<b>GPP_E21 Individual Voltage Select (GPPC_E21_VCCIO):</b>  0 = GPP_E21 Voltage set to 3.3v 1 = GPP_E21 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E21 GPIO pin.	Yes
	4	<b>GPP_E20 Individual Voltage Select (GPPC_E20_VCCIO):</b>  0 = GPP_E20 Voltage set to 3.3v 1 = GPP_E20 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E20 GPIO pin.	Yes
	3	<b>GPP_E19 Individual Voltage Select (GPPC_E19_VCCIO):</b>  0 = GPP_E19 Voltage set to 3.3v 1 = GPP_E19 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E19 GPIO pin.	Yes
	2	<b>GPP_E18 Individual Voltage Select (GPPC_E18_VCCIO):</b>  0 = GPP_E18 Voltage set to 3.3v 1 = GPP_E18 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E18 GPIO pin.	Yes
	1	<b>GPP_E17 Individual Voltage Select (GPPC_E17_VCCIO):</b>  0 = GPP_E17 Voltage set to 3.3v 1 = GPP_E17 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E17 GPIO pin.	Yes
	0	<b>GPP_E16 Individual Voltage Select (GPPC_E16_VCCIO):</b>  0 = GPP_E16 Voltage set to 3.3v 1 = GPP_E16 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_E16 GPIO pin.	Yes



## 9.13 PCH Descriptor Record 12 (Flash Descriptor Records)

Flash Address: FPSBA + 00Ch

Default Flash Address: 10Ch

Offset from 0	Bits	Description	Usage	FIT Visible
0x10Ch	7	<b>Intel® HD Audio Voltage Select (AZA_VCCIO):</b> 0 = Intel(R) HD Audio Voltage Select to 3.3v 1 = Intel(R) HD Audio Voltage Select set to 1.8v	This setting controls configures the VCCIO voltage for all of the Intel® HD Audio GPIO pins.	Yes
	6	Reserved, set to '0'		No
	5	<b>SLP_S5# / GDP10 Signal Configuration:</b> 0b = Use as SLP_S5# 1b = Use as GPD10		Yes
	4	<b>LAN PHY Power Control GPD11 Signal Configuration:</b> 0b = Use as LANPHYPC 1b = Use as GPD11  <b>Note:</b> 4. LANPHYPC can only be driven low if SLP_LAN# is deasserted. 5. Signal can instead be used as GPD11.	<b>LAN PHY Power Control:</b> LANPHYPC should be connected to LAN_DISABLE_N on the PHY. PCH will drive LANPHYPC. low to put the PHY into a low power state when functionality is not needed.	Yes
	3	<b>SLP_WLAN# / GPD9 Signal Configuration:</b> 0b = Use as SLP_WLAN# 1b = Use as GPD9	<b>LAN Sub-System Sleep Control:</b> When SLP_LAN# is de-asserted it indicates that the PHY device must be powered. When SLP_LAN# is asserted, power can be shut off to the PHY device. SLP_LAN# will always be deasserted in S0 and anytime SLP_A# is de-asserted.	Yes
	2	<b>SLP_A# / GPD6 Signal Configuration:</b> 0b = Use as SLP_A# 1b = Use as GPD6		Yes
	1	<b>SLP_S4# / GPD5 Signal Configuration:</b> 0b = Use as SLP_S4# 1b = Use as GPD5		Yes
	0	<b>SLP_S3# / GPD4 Signal Configuration:</b> 0b = Use as SLP_S3# 1b = Use as GPD4		Yes

## 9.14 PCH Descriptor Record 13 (Flash Descriptor Records)

Flash Address: FPSBA + 00Dh

Default Flash Address: 10Dh

Offset from 0	Bits	Description	Usage	FIT Visible
0x10Dh	7:0	Reserved, set to '0'		No





## 9.15 PCH Descriptor Record 14 (Flash Descriptor Records)

Flash Address: FPSBA + 00Eh

Default Flash Address: 10Eh

Offset from 0	Bits	Description	Usage	FIT Visible
0x10Eh	7:0	Reserved, set to '0'		No

## 9.16 PCH Descriptor Record 15 (Flash Descriptor Records)

Flash Address: FPSBA + 00Fh

Default Flash Address: 10Fh

Offset from 0	Bits	Description	Usage	FIT Visible
0x10Fh	7:0	Reserved, set to '0'		No

## 9.17 PCH Descriptor Record 16 (Flash Descriptor Records)

Flash Address: FPSBA + 010h

Default Flash Address: 110h

Offset from 0	Bits	Description	Usage	FIT Visible
0x110h	7:0	Reserved, set to '0'		No

## 9.18 PCH Descriptor Record 17 (Flash Descriptor Records)

Flash Address: FPSBA + 011h

Default Flash Address: 111h

Offset from 0	Bits	Description	Usage	FIT Visible
0x111h	7	GPP_D7 Individual Voltage Select (GPPC_D7_VCCIO):  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D7 GPIO pin.	Yes
	6	GPP_D6 Individual Voltage Select (GPPC_D6_VCCIO):  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D6 GPIO pin.	Yes



Offset from 0	Bits	Description	Usage	FIT Visible
0x111h (Cont)	5	<b>GPP_D5 Individual Voltage Select (GPPC_D5_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D5 GPIO pin.	Yes
	4	<b>GPP_D4 Individual Voltage Select (GPPC_D4_VCCIO):</b>  0 = GPP_D4 Voltage set to 3.3v 1 = GPP_D4 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D4 GPIO pin.	Yes
	3	<b>GPP_D3 Individual Voltage Select (GPPC_D3_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D3 GPIO pin.	Yes
	2	<b>GPP_D2 Individual Voltage Select (GPPC_D2_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D2 GPIO pin.	Yes
	1	<b>GPP_D1 Individual Voltage Select (GPPC_D1_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D1 GPIO pin.	Yes
	0	<b>GPP_D0 Individual Voltage Select (GPPC_D0_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D0 GPIO pin.	Yes

## 9.19 PCH Descriptor Record 18 (Flash Descriptor Records)

Flash Address: FPSBA + 012h

Default Flash Address: 112h

Offset from 0	Bits	Description	Usage	FIT Visible
0x112h	7	<b>GPP_D15 Individual Voltage Select (GPPC_D15_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D15 GPIO pin.	Yes
	6	<b>GPP_D14 Individual Voltage Select (GPPC_D14_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D14 GPIO pin.	Yes
	5	<b>GPP_D13 Individual Voltage Select (GPPC_D13_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D13 GPIO pin.	Yes



Offset from 0	Bits	Description	Usage	FIT Visible
0x112h (Cont)	4	<b>GPP_D12 Individual Voltage Select (GPPC_D12_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D12 GPIO pin.	Yes
	3	<b>GPP_D11 Individual Voltage Select (GPPC_D11_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D11 GPIO pin.	Yes
	2	<b>GPP_D10 Individual Voltage Select (GPPC_D10_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D10 GPIO pin.	Yes
	1	<b>GPP_D9 Individual Voltage Select (GPPC_D9_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D9 GPIO pin.	Yes
	0	<b>GPP_D8 Individual Voltage Select (GPPC_D8_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D8 GPIO pin.	Yes

## 9.20 PCH Descriptor Record 19 (Flash Descriptor Records)

Flash Address: FPSBA + 013h

Default Flash Address: 113h

Offset from 0	Bits	Description	Usage	FIT Visible
0x113h	7	<b>GPP_D23 Individual Voltage Select (GPPC_D23_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D23 GPIO pin.	Yes
	6	<b>GPP_D22 Individual Voltage Select (GPPC_D22_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D22 GPIO pin.	Yes
	5	<b>GPP_D21 Individual Voltage Select (GPPC_D21_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D21 GPIO pin.	Yes
	4	<b>GPP_D20 Individual Voltage Select (GPPC_D20_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D20 GPIO pin.	Yes



Offset from 0	Bits	Description	Usage	FIT Visible
0x113h (Cont)	3	<b>GPP_D19 Individual Voltage Select (GPPC_D19_VCCIO):</b> 0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D19 GPIO pin.	Yes
	2	<b>GPP_D18 Individual Voltage Select (GPPC_D18_VCCIO):</b> 0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D18 GPIO pin.	Yes
	1	<b>GPP_D17 Individual Voltage Select (GPPC_D17_VCCIO):</b> 0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D17 GPIO pin.	Yes
	0	<b>GPP_D16 Individual Voltage Select (GPPC_D16_VCCIO):</b> 0 = GPP_D16 Voltage set to 3.3v 1 = GPP_D16 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_D16 GPIO pin.	Yes

## 9.21 PCH Descriptor Record 20 (Flash Descriptor Records)

Flash Address: FPSBA + 014h

Default Flash Address: 114h

Offset from 0	Bits	Description	Usage	FIT Visible
0x114h	7	<b>GPP_H7 Individual Voltage Select (GPPC_H7_VCCIO):</b> 0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H7 GPIO pin.	Yes
	6	<b>GPP_H6 Individual Voltage Select (GPPC_H6_VCCIO):</b> 0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H6 GPIO pin.	Yes
	5	<b>GPP_H5 Individual Voltage Select (GPPC_H5_VCCIO):</b> 0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H5 GPIO pin.	Yes
	4	<b>GPP_H4 Individual Voltage Select (GPPC_H4_VCCIO):</b> 0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H4 GPIO pin.	Yes
	3	<b>GPP_H3 Individual Voltage Select (GPPC_H3_VCCIO):</b> 0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H3 GPIO pin.	Yes



Offset from 0	Bits	Description	Usage	FIT Visible
0x114h (Cont)	2	<b>GPP_H2 Individual Voltage Select (GPPC_H2_VCCIO):</b> 0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H2 GPIO pin.	Yes
	1	<b>GPP_H1 Individual Voltage Select (GPPC_H1_VCCIO):</b> 0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H1 GPIO pin.	Yes
	0	<b>GPP_H0 Individual Voltage Select (GPPC_H0_VCCIO):</b> 0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H0 GPIO pin.	Yes

## 9.22 PCH Descriptor Record 21 (Flash Descriptor Records)

Flash Address: FPSBA + 015h

Default Flash Address: 115h

Offset from 0	Bits	Description	Usage	FIT Visible
0x115h	7	<b>GPP_H15 Individual Voltage Select (GPPC_H15_VCCIO):</b> 0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H15 GPIO pin.	Yes
	6	<b>GPP_H14 Individual Voltage Select (GPPC_H14_VCCIO):</b> 0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H14 GPIO pin.	Yes
	5	<b>GPP_H13 Individual Voltage Select (GPPC_H13_VCCIO):</b> 0 = GPP_H13 Voltage set to 3.3v 1 = GPP_H13 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H13 GPIO pin.	Yes
	4	<b>GPP_H12 Individual Voltage Select (GPPC_H12_VCCIO):</b> 0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H12 GPIO pin.	Yes
	3	<b>GPP_H11 Individual Voltage Select (GPPC_H11_VCCIO):</b> 0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H11 GPIO pin.	Yes
	2	<b>GPP_H10 Individual Voltage Select (GPPC_H10_VCCIO):</b> 0 = GPP_H10 Voltage set to 3.3v 1 = GPP_H10 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H10 GPIO pin.	Yes



Offset from 0	Bits	Description	Usage	FIT Visible
0x115h (Cont)	1	<b>GPP_H9 Individual Voltage Select (GPPC_H9_VCCIO):</b>  0 = GPP_H9 Voltage set to 3.3v 1 = GPP_H9 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H9 GPIO pin.	Yes
	0	<b>GPP_H8 Individual Voltage Select (GPPC_H8_VCCIO):</b>  0 = GPP_H8 Voltage set to 3.3v 1 = GPP_H8 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H8 GPIO pin.	Yes

## 9.23 PCH Descriptor Record 22 (Flash Descriptor Records)

Flash Address: FPSBA + 016h

Default Flash Address: 116h

Offset from 0	Bits	Description	Usage	FIT Visible
0x116h	7	<b>GPP_H23 Individual Voltage Select (GPPC_H23_VCCIO):</b>  0 = GPP_H23 Voltage set to 3.3v 1 = GPP_H23 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H23 GPIO pin.	Yes
	6	<b>GPP_H22 Individual Voltage Select (GPPC_H22_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H22 GPIO pin.	Yes
	5	<b>GPP_H21 Individual Voltage Select (GPPC_H21_VCCIO):</b>  0 = GPP_H21 Voltage set to 3.3v 1 = GPP_H21 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H21 GPIO pin.	Yes
	4	<b>GPP_H20 Individual Voltage Select (GPPC_H20_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H20 GPIO pin.	Yes
	3	<b>GPP_H19 Individual Voltage Select (GPPC_H19_VCCIO):</b>  0 = GPP_H19 Voltage set to 3.3v 1 = GPP_H19 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H19 GPIO pin.	Yes
	2	<b>GPP_H18 Individual Voltage Select (GPPC_H18_VCCIO):</b>  0 = GPP_H18 Voltage set to 3.3v 1 = GPP_H18 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H18 GPIO pin.	Yes
	1	<b>GPP_H17 Individual Voltage Select (GPPC_H17_VCCIO):</b>  0 = GPP_H17 Voltage set to 3.3v 1 = GPP_H17 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H17 GPIO pin.	Yes



Offset from 0	Bits	Description	Usage	FIT Visible
0x116h (Cont)	0	<b>GPP_H16 Individual Voltage Select (GPPC_H16_VCCIO):</b>  0 = GPP_H16 Voltage set to 3.3v 1 = GPP_H16 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_H16 GPIO pin.	Yes

## 9.24 PCH Descriptor Record 23 (Flash Descriptor Records)

Flash Address: FPSBA + 017h

Default Flash Address: 117h

Offset from 0	Bits	Description	Usage	FIT Visible
0x117h	7:0	Reserved, set to '0'		No

## 9.25 PCH Descriptor Record 24 (Flash Descriptor Records)

Flash Address: FPSBA + 018h

Default Flash Address: 118h

Offset from 0	Bits	Description	Usage	FIT Visible
0x118h	7:0	Reserved, set to '0'		No

## 9.26 PCH Descriptor Record 25 (Flash Descriptor Records)

Flash Address: FPSBA + 019h

Default Flash Address: 119h

Offset from 0	Bits	Description	Usage	FIT Visible
0x119h	7	<b>GPP_A7 Individual Voltage Select (GPPC_A7_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A7 GPIO pin.	Yes
	6	<b>GPP_A6 Individual Voltage Select (GPPC_A6_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A6 GPIO pin.	Yes
	5	<b>GPP_A5 Individual Voltage Select (GPPC_A5_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A5 GPIO pin.	Yes



Offset from 0	Bits	Description	Usage	FIT Visible
0x119h (Cont)	4	<b>GPP_A4 Individual Voltage Select (GPPC_A4_VCCIO):</b> 0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A4 GPIO pin.	Yes
	3	<b>GPP_A3 Individual Voltage Select (GPPC_A3_VCCIO):</b> 0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A3 GPIO pin.	Yes
	2	<b>GPP_A2 Individual Voltage Select (GPPC_A2_VCCIO):</b> 0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A2 GPIO pin.	Yes
	1	<b>GPP_A1 Individual Voltage Select (GPPC_A1_VCCIO):</b> 0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A1 GPIO pin.	Yes
	0	<b>GPP_A0 Individual Voltage Select (GPPC_A0_VCCIO):</b> 0 = GPP_A0 Voltage set to 3.3v 1 = GPP_A0 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A0 GPIO pin.	Yes

## 9.27 PCH Descriptor Record 26 (Flash Descriptor Records)

Flash Address: FPSBA + 01Ah

Default Flash Address: 11Ah

Offset from 0	Bits	Description	Usage	FIT Visible
0x11Ah	7	<b>GPP_A15 Individual Voltage Select (GPPC_A15_VCCIO):</b> 0 = GPP_A15 Voltage set to 3.3v 1 = GPP_A15 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A15 GPIO pin.	Yes
	6	<b>GPP_A14 Individual Voltage Select (GPPC_A14_VCCIO):</b> 0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A14 GPIO pin.	Yes
	5	<b>GPP_A13 Individual Voltage Select (GPPC_A13_VCCIO):</b> 0 = GPP_A13 Voltage set to 3.3v 1 = GPP_A13 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A13 GPIO pin.	Yes
	4	<b>GPP_A12 Individual Voltage Select (GPPC_A12_VCCIO):</b> 0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A12 GPIO pin.	Yes





Offset from 0	Bits	Description	Usage	FIT Visible
0x11Ah (Cont)	3	<b>GPP_A11 Individual Voltage Select (GPPC_A11_VCCIO):</b>  0 = GPP_A11 Voltage set to 3.3v 1 = GPP_A11 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A11 GPIO pin.	Yes
	2	<b>GPP_A10 Individual Voltage Select (GPPC_A10_VCCIO):</b>  0 = GPP_A10 Voltage set to 3.3v 1 = GPP_A10 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A10 GPIO pin.	Yes
	1	<b>GPP_A9 Individual Voltage Select (GPPC_A9_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A9 GPIO pin.	Yes
	0	<b>GPP_A8 Individual Voltage Select (GPPC_A8_VCCIO):</b>  0 = GPP_A8 Voltage set to 3.3v 1 = GPP_A8 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A8 GPIO pin.	Yes

## 9.28 PCH Descriptor Record 27 (Flash Descriptor Records)

Flash Address: FPSBA + 01Bh

Default Flash Address: 11Bh

Offset from 0	Bits	Description	Usage	FIT Visible
0x11Bh	7	<b>GPP_A23 Individual Voltage Select (GPPC_A23_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A23 GPIO pin.	Yes
	6	<b>GPP_A22 Individual Voltage Select (GPPC_A22_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A22 GPIO pin.	Yes
	5	<b>GPP_A21 Individual Voltage Select (GPPC_A21_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A21 GPIO pin.	Yes
	4	<b>GPP_A20 Individual Voltage Select (GPPC_A20_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A20 GPIO pin.	Yes
	3	<b>GPP_A19 Individual Voltage Select (GPPC_A19_VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A19 GPIO pin.	Yes



Offset from 0	Bits	Description	Usage	FIT Visible
0x11Bh (Cont)	2	<b>GPP_A18 Individual Voltage Select (GPPC_A18 VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A18 GPIO pin.	Yes
	1	<b>GPP_A17 Individual Voltage Select (GPPC_A17 VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A17 GPIO pin.	Yes
	0	<b>GPP_A16 Individual Voltage Select (GPPC_A16 VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_A16 GPIO pin.	Yes

## 9.29 PCH Descriptor Record 28 (Flash Descriptor Records)

Flash Address: FPSBA + 01Ch

Default Flash Address: 11Ch

Offset from 0	Bits	Description	Usage	FIT Visible
0x11Ch	7	<b>GPP_B7 Individual Voltage Select (GPPC_B7 VCCIO):</b>  0 = GPP_B7 Voltage set to 3.3v 1 = GPP_B7 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B7 GPIO pin.	Yes
	6	<b>GPP_B6 Individual Voltage Select (GPPC_B6 VCCIO):</b>  0 = GPP_B6 Voltage set to 3.3v 1 = GPP_B6 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B6 GPIO pin.	Yes
	5	<b>GPP_B5 Individual Voltage Select (GPPC_B5 VCCIO):</b>  0 = GPP_B5 Voltage set to 3.3v 1 = GPP_B5 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B5 GPIO pin.	Yes
	4	<b>GPP_B4 Individual Voltage Select (GPPC_B4 VCCIO):</b>  0 = GPP_B4 Voltage set to 3.3v 1 = GPP_B4 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B4 GPIO pin.	Yes
	3	<b>GPP_B3 Individual Voltage Select (GPPC_B3 VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B3 GPIO pin.	Yes



Offset from 0	Bits	Description	Usage	FIT Visible
0x11Ch (Cont)	2	<b>GPP_B2 Individual Voltage Select (GPPC_B2 VCCIO):</b>  0 = GPP_B2 Voltage set to 3.3v 1 = GPP_B2 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B2 GPIO pin.	Yes
	1	<b>GPP_B1 Individual Voltage Select (GPPC_B1 VCCIO):</b>  0 = GPP_B1 Voltage set to 3.3v 1 = GPP_B1 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B1 GPIO pin.	Yes
	0	<b>GPP_B0 Individual Voltage Select (GPPC_B0 VCCIO):</b>  0 = GPP_B0 Voltage set to 3.3v 1 = GPP_B0 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B0 GPIO pin.	Yes

## 9.30 PCH Descriptor Record 29 (Flash Descriptor Records)

Flash Address: FPSBA + 01Dh

Default Flash Address: 11Dh

Offset from 0	Bits	Description	Usage	FIT Visible
0x11Dh	7	<b>GPP_B15 Individual Voltage Select (GPPC_B15 VCCIO):</b>  0 = GPP_B15 Voltage set to 3.3v 1 = GPP_B15 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B15 GPIO pin.	Yes
	6	<b>GPP_B14 Individual Voltage Select (GPPC_B14 VCCIO):</b>  0 = GPP_B14 Voltage set to 3.3v 1 = GPP_B14 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B14 GPIO pin.	Yes
	5	<b>GPP_B13 Individual Voltage Select (GPPC_B13 VCCIO):</b>  0 = GPP_B13 Voltage set to 3.3v 1 = GPP_B13 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B13 GPIO pin.	Yes
	4	<b>GPP_B12 Individual Voltage Select (GPPC_B12 VCCIO):</b>  0 = GPP_B12 Voltage set to 3.3v 1 = GPP_B12 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B12 GPIO pin.	Yes
	3	<b>GPP_B11 Individual Voltage Select (GPPC_B11 VCCIO):</b>  0 = GPP_B11 Voltage set to 3.3v 1 = GPP_B11 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B11 GPIO pin.	Yes



Offset from 0	Bits	Description	Usage	FIT Visible
0x11Dh (Cont)	2	<b>GPP_B10 Individual Voltage Select (GPPC_B10 VCCIO):</b>  0 = GPP_B10 Voltage set to 3.3v 1 = GPP_B10 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B10 GPIO pin.	Yes
	1	<b>GPP_B9 Individual Voltage Select (GPPC_B9 VCCIO):</b>  0 = GPP_B9 Voltage set to 3.3v 1 = GPP_B9 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B9 GPIO pin.	Yes
	0	<b>GPP_B8 Individual Voltage Select (GPPC_B8 VCCIO):</b>  0 = GPP_B8 Voltage set to 3.3v 1 = GPP_B8 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B8 GPIO pin.	Yes

## 9.31 PCH Descriptor Record 30 (Flash Descriptor Records)

Flash Address: FPSBA + 01Eh

Default Flash Address: 11Eh

Offset from 0	Bits	Description	Usage	FIT Visible
0x11Eh	7	<b>GPP_B23 Individual Voltage Select (GPPC_B23 VCCIO):</b>  0 = GPP_B23 Voltage set to 3.3v 1 = GPP_B23 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B23 GPIO pin.	Yes
	6	<b>GPP_B22 Individual Voltage Select (GPPC_B22 VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B22 GPIO pin.	Yes
	5	<b>GPP_B21 Individual Voltage Select (GPPC_B21 VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B21 GPIO pin.	Yes
	4	<b>GPP_B20 Individual Voltage Select (GPPC_B20 VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B20 GPIO pin.	Yes
	3	<b>GPP_B19 Individual Voltage Select (GPPC_B19 VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B19 GPIO pin.	Yes



Offset from 0	Bits	Description	Usage	FIT Visible
0x11Eh (Cont)	2	<b>GPP_B18 Individual Voltage Select (GPPC_B18 VCCIO):</b>  0 = GPP_B18 Voltage set to 3.3v 1 = GPP_B18 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B18 GPIO pin.	Yes
	1	<b>GPP_B17 Individual Voltage Select (GPPC_B17 VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B17 GPIO pin.	Yes
	0	<b>GPP_B16 Individual Voltage Select (GPPC_B16 VCCIO):</b>  0 = GPP_D3 Voltage set to 3.3v 1 = GPP_D3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_B16 GPIO pin.	Yes

## 9.32 PCH Descriptor Record 31 (Flash Descriptor Records)

Flash Address: FPSBA + 01Fh

Default Flash Address: 11Fh

Offset from 0	Bits	Description	Usage	FIT Visible
0x11Fh	7	<b>GPP_G7 Individual Voltage Select (GPPC_G7 VCCIO):</b>  0 = GPP_G7 Voltage set to 3.3v 1 = GPP_G7 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_G7 GPIO pin.	Yes
	6	<b>GPP_G6 Individual Voltage Select (GPPC_G6 VCCIO):</b>  0 = GPP_G6 Voltage set to 3.3v 1 = GPP_G6 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_G6 GPIO pin.	Yes
	5	<b>GPP_G5 Individual Voltage Select (GPPC_G5 VCCIO):</b>  0 = GPP_G5 Voltage set to 3.3v 1 = GPP_G5 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_G5 GPIO pin.	Yes
	4	<b>GPP_G4 Individual Voltage Select (GPPC_G4 VCCIO):</b>  0 = GPP_G4 Voltage set to 3.3v 1 = GPP_G4 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_G4 GPIO pin.	Yes
	3	<b>GPP_G3 Individual Voltage Select (GPPC_G3 VCCIO):</b>  0 = GPP_G3 Voltage set to 3.3v 1 = GPP_G3 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_G3 GPIO pin.	Yes



Offset from 0	Bits	Description	Usage	FIT Visible
0x11Fh (Cont)	2	<b>GPP_G2 Individual Voltage Select (GPPC_G2 VCCIO):</b>  0 = GPP_G2 Voltage set to 3.3v 1 = GPP_G2 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_G2 GPIO pin.	Yes
	1	<b>GPP_G1 Individual Voltage Select (GPPC_G1 VCCIO):</b>  0 = GPP_G1 Voltage set to 3.3v 1 = GPP_G1 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_G1 GPIO pin.	Yes
	0	<b>GPP_G0 Individual Voltage Select (GPPC_G0 VCCIO):</b>  0 = GPP_G0 Voltage set to 3.3v 1 = GPP_G0 Voltage set to 1.8v	This setting controls the VCCIO voltage for the GPP_G0 GPIO pin.	Yes

## 9.33 PCH Descriptor Record 32 (Flash Descriptor Records)

Flash Address: FPSBA + 020h

Default Flash Address: 120h

Offset from 0	Bits	Description	Usage	FIT Visible
0x120h	7:6	Reserved, set to '0'		No
	5	<b>XHCI Port 6 Ownership Strap (XHC_PORT6_OWNERSHIP_STRAP):</b> Strap to decide XHCI Port 6 Ownership between XHCI/PCIe/CSI.  0x0 = XHC Port 6 configured as XHC 0x1 = XHC Port 6 configured as Non-XHC	This strap must also be configured when setting the USB3 / PCIe Combo Port 5 (FIA/PCIE_USB3_P5_STRP).  <b>Note:</b> When <b>USB3 / PCIe Combo Port 5 (FIA/PCIE_USB3_P5_STRP)</b> configured as USB3 this setting needs to be set to 0x0. When <b>USB3 / PCIe Combo Port 5 (FIA/PCIE_USB3_P5_STRP)</b> is configured as PCIe this setting needs to be set to 0x1.	No
	4	<b>XHCI Port 5 Ownership Strap (XHC_PORT5_OWNERSHIP_STRAP):</b> Strap to decide XHCI Port 5 Ownership between XHCI/PCIe/CSI.  0x0 = XHC Port 5 configured as XHC 0x1 = XHC Port 5 configured as Non-XHC	This strap must also be configured when setting the USB3 / PCIe Combo Port 4 (FIA/PCIE_USB3_P4_STRP).  <b>Note:</b> When <b>USB3 / PCIe Combo Port 4 (FIA/PCIE_USB3_P4_STRP)</b> configured as USB3 this setting needs to be set to 0x0. When <b>USB3 / PCIe Combo Port 4 (FIA/PCIE_USB3_P4_STRP)</b> is configured as PCIe this setting needs to be set to 0x1.	No
	3	<b>XHCI Port 4 Ownership Strap (XHC_PORT4_OWNERSHIP_STRAP):</b> Strap to decide XHCI Port 4 Ownership between XHCI/PCIe/CSI.  0x0 = XHC Port 4 configured as XHC 0x1 = XHC Port 4 configured as Non-XHC	This strap must also be configured when setting the USB3 / PCIe Combo Port 3 (FIA/PCIE_USB3_P3_STRP).  <b>Note:</b> When <b>USB3 / PCIe Combo Port 3 (FIA/PCIE_USB3_P3_STRP)</b> configured as USB3 this setting needs to be set to 0x0. When <b>USB3 / PCIe Combo Port 3 (FIA/PCIE_USB3_P3_STRP)</b> is configured as PCIe this setting needs to be set to 0x1.	No



Offset from 0	Bits	Description	Usage	FIT Visible
0x120h (Cont)	2	<b>XHCI Port 3 Ownership Strap (XHC_PORT3_OWNERSHIP_STRAP):</b> Strap to decide XHCI Port 3 Ownership between XHCI/PCIe/CSI.  0x0 = XHC Port 3 configured as XHC 0x1 = XHC Port 3 configures as Non-XHC	This strap must also be configured when setting the USB3 / PCIe Combo Port 2 (FIA/PCIE_USB3_P2_STRP).  <b>Note:</b> When <b>USB3 / PCIe Combo Port 2 (FIA/PCIE_USB3_P2_STRP)</b> configured as USB3 this setting needs to be set to 0x0. When <b>USB3 / PCIe Combo Port 2 (FIA/PCIE_USB3_P2_STRP)</b> is configured as PCIe this setting needs to be set to 0x1.	No
	1	<b>XHCI Port 2 Ownership Strap (XHC_PORT2_OWNERSHIP_STRAP):</b> Strap to decide XHCI Port 2 Ownership between XHCI/PCIe/CSI.  0x0 = XHC Port 2 configured as XHC 0x1 = XHC Port 2 configures as Non-XHC	This strap must also be configured when setting the USB3 / PCIe Combo Port 1 (FIA/PCIE_USB3_P1_STRP).  <b>Note:</b> When <b>USB3 / PCIe Combo Port 1 (FIA/PCIE_USB3_P1_STRP)</b> configured as USB3 this setting needs to be set to 0x0. When <b>USB3 / PCIe Combo Port 1 (FIA/PCIE_USB3_P1_STRP)</b> is configured as PCIe this setting needs to be set to 0x1.	No
	0	<b>XHCI Port 1 Ownership Strap (XHC_PORT1_OWNERSHIP_STRAP):</b> Strap to decide XHCI Port 1 Ownership between XHCI/PCIe/CSI.  0x0 = XHC Port 1 configured as XHC 0x1 = XHC Port 1 configures as Non-XHC	This strap must also be configured when setting the USB3 / PCIe Combo Port 0 (FIA/PCIE_USB3_P0_STRP).  <b>Note:</b> When <b>USB3 / PCIe Combo Port 0 (FIA/PCIE_USB3_P0_STRP)</b> configured as USB3 this setting needs to be set to 0x0. When <b>USB3 / PCIe Combo Port 0 (FIA/PCIE_USB3_P0_STRP)</b> is configured as PCIe this setting needs to be set to 0x1.	No

## 9.34 PCH Descriptor Record 33 (Flash Descriptor Records)

Flash Address: FPSBA + 021h

Default Flash Address: 121h

Offset from 0	Bits	Description	Usage	FIT Visible
0x121h	7:0	Reserved, set to '0'		No



## 9.35 PCH Descriptor Record 34 (Flash Descriptor Records)

Flash Address: FPSBA + 022h

Default Flash Address: 122h

Offset from 0	Bits	Description	Usage	FIT Visible
0x122h	7:6	Reserved, set to '0'		No
	5	<b>USB3 Port 6 Speed Select:</b> 0 = Port 6 is configured as USB3.1 Gen2 1 = Port 6 is configured as USB3.1 Gen1	This setting determines the USB3 Port 6 speed capabilities.	Yes
	4	<b>USB3 Port 5 Speed Select:</b> 0 = Port 5 is configured as USB3.1 Gen2 1 = Port 5 is configured as USB3.1 Gen1	This setting determines the USB3 Port 5 speed capabilities.	Yes
	3	<b>USB3 Port 4 Speed Select:</b> 0 = Port 4 is configured as USB3.1 Gen2 1 = Port 4 is configured as USB3.1 Gen1	This setting determines the USB3 Port 4 speed capabilities.	Yes
	2	<b>USB3 Port 3 Speed Select:</b> 0 = Port 3 is configured as USB3.1 Gen2 1 = Port 3 is configured as USB3.1 Gen1	This setting determines the USB3 Port 3 speed capabilities.	Yes
	1	<b>USB3 Port 2 Speed Select:</b> 0 = Port 2 is configured as USB3.1 Gen2 1 = Port 2 is configured as USB3.1 Gen1	This setting determines the USB3 Port 2 speed capabilities.	Yes
	0	<b>USB3 Port 1 Speed Select:</b> 0 = Port 1 is configured as USB3.1 Gen2 1 = Port 1 is configured as USB3.1 Gen1	This setting determines the USB3 Port 1 speed capabilities.	Yes





## 9.36 PCH Descriptor Record 35 (Flash Descriptor Records)

Flash Address: FPSBA + 023h

Default Flash Address: 123h

Offset from 0	Bits	Description	Usage	FIT Visible
0x123h	7:6	Reserved, set to '0'		No
	5	<b>USB3 Port 6 Initialization Speed Select:</b> 0 = Port 6 will boot as USB 3.1 Gen1 and carry on LBPM if USB 3.1 is Gen2 enabled 1 = Port 6 will boot as USB 3.1 Gen2 and skip LBPM	This setting determines USB3 Port 6 speed during platform power-up.	Yes
	4	<b>USB3 Port 5 Initialization Speed Select:</b> 0 = Port 5 will boot as USB 3.1 Gen1 and carry on LBPM if USB 3.1 is Gen2 enabled 1 = Port 5 will boot as USB 3.1 Gen2 and skip LBPM	This setting determines USB3 Port 5 speed during platform power-up.	Yes
	3	<b>USB3 Port 4 Initialization Speed Select:</b> 0 = Port 4 will boot as USB 3.1 Gen1 and carry on LBPM if USB 3.1 is Gen2 enabled 1 = Port 4 will boot as USB 3.1 Gen2 and skip LBPM	This setting determines USB3 Port 4 speed during platform power-up.	Yes
	2	<b>USB3 Port 3 Initialization Speed Select:</b> 0 = Port 3 will boot as USB 3.1 Gen1 and carry on LBPM if USB 3.1 is Gen2 enabled 1 = Port 3 will boot as USB 3.1 Gen2 and skip LBPM	This setting determines USB3 Port 3 speed during platform power-up.	Yes
	1	<b>USB3 Port 2 Initialization Speed Select:</b> 0 = Port 2 will boot as USB 3.1 Gen1 and carry on LBPM if USB 3.1 is Gen2 enabled 1 = Port 2 will boot as USB 3.1 Gen2 and skip LBPM	This setting determines USB3 Port 2 speed during platform power-up.	Yes
	0	<b>USB3 Port 1 Initialization Speed Select:</b> 0 = Port 1 will boot as USB 3.1 Gen1 and carry on LBPM if USB 3.1 is Gen2 enabled 1 = Port 1 will boot as USB 3.1 Gen2 and skip LBPM	This setting determines USB3 Port 1 speed during platform power-up.	Yes



## 9.37 PCH Descriptor Record 36 (Flash Descriptor Records)

Flash Address: FPSBA + 024h

Default Flash Address: 124h

Offset from 0	Bits	Description	Usage	FIT Visible
0x124h	7:4	<b>USB3 Port 2 Connector Type Select:</b> 0x0 = USB Port 1 connector set to Type C 0x1 = USB Port 1 connector set to Micro AB 0x2 = USB Port 1 connector set to Type A 0x3 = USB Port 1 connector set to Type B 0x4 = USB Port 1 connector set to Express Card / M.2 S2	This setting configures the physical connector type for where the USB port [Super Speed / Enhanced Super Speed] is routed.	Yes
	3:0	<b>USB3 Port 1 Connector Type Select:</b> 0x0 = USB Port 1 connector set to Type C 0x1 = USB Port 1 connector set to Micro AB 0x2 = USB Port 1 connector set to Type A 0x3 = USB Port 1 connector set to Type B 0x4 = USB Port 1 connector set to Express Card / M.2 S2	This setting configures the physical connector type for where the USB port [Super Speed / Enhanced Super Speed] is routed.	Yes

## 9.38 PCH Descriptor Record 37 (Flash Descriptor Records)

Flash Address: FPSBA + 025h

Default Flash Address: 125h

Offset from 0	Bits	Description	Usage	FIT Visible
0x125h	7:4	<b>USB3 Port 4 Connector Type Select:</b> 0x0 = USB Port 1 connector set to Type C 0x1 = USB Port 1 connector set to Micro AB 0x2 = USB Port 1 connector set to Type A 0x3 = USB Port 1 connector set to Type B 0x4 = USB Port 1 connector set to Express Card / M.2 S2	This setting configures the physical connector type for where the USB port [Super Speed / Enhanced Super Speed] is routed.	Yes
	3:0	<b>USB3 Port 3 Connector Type Select:</b> 0x0 = USB Port 1 connector set to Type C 0x1 = USB Port 1 connector set to Micro AB 0x2 = USB Port 1 connector set to Type A 0x3 = USB Port 1 connector set to Type B 0x4 = USB Port 1 connector set to Express Card / M.2 S2	This setting configures the physical connector type for where the USB port [Super Speed / Enhanced Super Speed] is routed.	Yes



## 9.39 PCH Descriptor Record 38 (Flash Descriptor Records)

Flash Address: FPSBA + 026h

Default Flash Address: 126h

Offset from 0	Bits	Description	Usage	FIT Visible
0x126h	7:4	<b>USB3 Port 6 Connector Type Select:</b> 0x0 = USB Port 1 connector set to Type C 0x1 = USB Port 1 connector set to Micro AB 0x2 = USB Port 1 connector set to Type A 0x3 = USB Port 1 connector set to Type B 0x4 = USB Port 1 connector set to Express Card / M.2 S2	This setting configures the physical connector type for where the USB port [Super Speed / Enhanced Super Speed] is routed.	Yes
	3:0	<b>USB3 Port 5 Connector Type Select:</b> 0x0 = USB Port 1 connector set to Type C 0x1 = USB Port 1 connector set to Micro AB 0x2 = USB Port 1 connector set to Type A 0x3 = USB Port 1 connector set to Type B 0x4 = USB Port 1 connector set to Express Card / M.2 S2	This setting configures the physical connector type for where the USB port [Super Speed / Enhanced Super Speed] is routed.	Yes

## 9.40 PCH Descriptor Record 39 (Flash Descriptor Records)

Flash Address: FPSBA + 027h

Default Flash Address: 127h

Offset from 0	Bits	Description	Usage	FIT Visible
0x127h	7:4	<b>USB2 Port 2 Connector Type Select:</b> 0x0 = USB Port 1 connector set to Type C 0x1 = USB Port 1 connector set to Micro AB 0x2 = USB Port 1 connector set to Type A 0x3 = USB Port 1 connector set to Type B 0x4 = USB Port 1 connector set to Express Card / M.2 S2	This setting configures the USB2 Port 2 physical connector type for where the USB port is routed.	Yes
	3:0	<b>USB2 Port 1 Connector Type Select:</b> 0x0 = USB Port 1 connector set to Type C 0x1 = USB Port 1 connector set to Micro AB 0x2 = USB Port 1 connector set to Type A 0x3 = USB Port 1 connector set to Type B 0x4 = USB Port 1 connector set to Express Card / M.2 S2	This setting configures the USB2 Port 1 physical connector type for where the USB port is routed.	Yes



## 9.41 PCH Descriptor Record 40 (Flash Descriptor Records)

Flash Address: FPSBA + 028h

Default Flash Address: 128h

Offset from 0	Bits	Description	Usage	FIT Visible
0x128h	7:4	<b>USB2 Port 4 Connector Type Select:</b> 0x0 = USB Port 1 connector set to Type C 0x1 = USB Port 1 connector set to Micro AB 0x2 = USB Port 1 connector set to Type A 0x3 = USB Port 1 connector set to Type B 0x4 = USB Port 1 connector set to Express Card / M.2 S2	This setting configures the USB2 Port 4 physical connector type for where the USB port is routed.	Yes
	3:0	<b>USB2 Port 3 Connector Type Select:</b> 0x0 = USB Port 1 connector set to Type C 0x1 = USB Port 1 connector set to Micro AB 0x2 = USB Port 1 connector set to Type A 0x3 = USB Port 1 connector set to Type B 0x4 = USB Port 1 connector set to Express Card / M.2 S2	This setting configures the USB2 Port 3 physical connector type for where the USB port is routed.	Yes

## 9.42 PCH Descriptor Record 41 (Flash Descriptor Records)

Flash Address: FPSBA + 029h

Default Flash Address: 129h

Offset from 0	Bits	Description	Usage	FIT Visible
0x129h	7:4	<b>USB2 Port 6 Connector Type Select:</b> 0x0 = Reserved 0x1 = USB Port 1 connector set to Micro AB 0x2 = USB Port 1 connector set to Type A 0x3 = USB Port 1 connector set to Type B 0x4 = USB Port 1 connector set to Express Card / M.2 S2	This setting configures the USB2 Port 6 physical connector type for where the USB port is routed.	Yes
	3:0	<b>USB2 Port 5 Connector Type Select:</b> 0x0 = Reserved 0x1 = USB Port 1 connector set to Micro AB 0x2 = USB Port 1 connector set to Type A 0x3 = USB Port 1 connector set to Type B 0x4 = USB Port 1 connector set to Express Card / M.2 S2	This setting configures the USB2 Port 5 physical connector type for where the USB port is routed.	Yes



## 9.43 PCH Descriptor Record 42 (Flash Descriptor Records)

Flash Address: FPSBA + 02Ah

Default Flash Address: 12Ah

Offset from 0	Bits	Description	Usage	FIT Visible
0x12Ah	7:4	<b>USB2 Port 8 Connector Type Select:</b> 0x0 = Reserved 0x1 = USB Port 1 connector set to Micro AB 0x2 = USB Port 1 connector set to Type A 0x3 = USB Port 1 connector set to Type B 0x4 = USB Port 1 connector set to Express Card / M.2 S2	This setting configures the USB2 Port 8 physical connector type for where the USB port is routed.	Yes
	3:0	<b>USB2 Port 7 Connector Type Select:</b> 0x0 = Reserved 0x1 = USB Port 1 connector set to Micro AB 0x2 = USB Port 1 connector set to Type A 0x3 = USB Port 1 connector set to Type B 0x4 = USB Port 1 connector set to Express Card / M.2 S2	This setting configures the USB2 Port 7 physical connector type for where the USB port is routed.	Yes

## 9.44 PCH Descriptor Record 43 (Flash Descriptor Records)

Flash Address: FPSBA + 02Bh

Default Flash Address: 12Bh

Offset from 0	Bits	Description	Usage	FIT Visible
0x12Bh	7:4	<b>USB2 Port 10 Connector Type Select:</b> 0x0 = Reserved 0x1 = USB Port 1 connector set to Micro AB 0x2 = USB Port 1 connector set to Type A 0x3 = USB Port 1 connector set to Type B 0x4 = USB Port 1 connector set to Express Card / M.2 S2	This setting configures the USB2 Port 10 physical connector type for where the USB port is routed.	Yes
	3:0	<b>USB2 Port 9 Connector Type Select:</b> 0x0 = Reserved 0x1 = USB Port 1 connector set to Micro AB 0x2 = USB Port 1 connector set to Type A 0x3 = USB Port 1 connector set to Type B 0x4 = USB Port 1 connector set to Express Card / M.2 S2	This setting configures the USB2 Port 9 physical connector type for where the USB port is routed.	Yes

## 9.45 PCH Descriptor Record 44 (Flash Descriptor Records)

Flash Address: FPSBA + 02Ch

Default Flash Address: 12Ch

Offset from 0	Bits	Description	Usage	FIT Visible
0x12Ch	7:0	Reserved, set to '0x22'		No



## 9.46 PCH Descriptor Record 45 (Flash Descriptor Records)

Flash Address: FPSBA + 02Dh

Default Flash Address: 12Dh

Offset from 0	Bits	Description	Usage	FIT Visible
0x12Dh	7:1	Reserved, set to '0'		No
	0	<b>USB Type AB mode Select:</b> 0 = USB Type AB connector switches based on SW event 1 = USB Type AB connector switches based on HW event	This setting configures the mode for the USB Type AB connector.	Yes

## 9.47 PCH Descriptor Record 46 (Flash Descriptor Records)

Flash Address: FPSBA + 02Eh

Default Flash Address: 12Eh

Offset from 0	Bits	Description	Usage	FIT Visible
0x12Eh	7:0	Reserved, set to '0'		No

## 9.48 PCH Descriptor Record 47 (Flash Descriptor Records)

Flash Address: FPSBA + 02Fh

Default Flash Address: 12Fh

Offset from 0	Bits	Description	Usage	FIT Visible
0x12Fh	7:0	Reserved, set to '0'		No

## 9.49 PCH Descriptor Record 48 (Flash Descriptor Records)

Flash Address: FPSBA + 030h

Default Flash Address: 130h

Offset from 0	Bits	Description	Usage	FIT Visible
0x130h	7	Reserved, set to '0'		No
	6	Reserved, set to '0x1'		No
	5:0	Reserved, set to '0x7'		No



## 9.50 PCH Descriptor Record 49 (Flash Descriptor Records)

Flash Address: FPSBA + 031h

Default Flash Address: 131h

Offset from 0	Bits	Description	Usage	FIT Visible
0x131h	23:0	Reserved, set to '0'		No

## 9.51 PCH Descriptor Record 50 (Flash Descriptor Records)

Flash Address: FPSBA + 034h

Default Flash Address: 134h

Offset from 0	Bits	Description	Usage	FIT Visible
0x134h	15:0	Reserved, set to '0'		No

## 9.52 PCH Descriptor Record 51 (Flash Descriptor Records)

Flash Address: FPSBA + 036h

Default Flash Address: 136h

Offset from 0	Bits	Description	Usage	FIT Visible
0x136h	7:0	Reserved, set to '0xff'		No

## 9.53 PCH Descriptor Record 52 (Flash Descriptor Records)

Flash Address: FPSBA + 037h

Default Flash Address: 137h

Offset from 0	Bits	Description	Usage	FIT Visible
0x137h	7:0	Reserved, set to '0'		No



## 9.54 PCH Descriptor Record 53 (Flash Descriptor Records)

Flash Address: FPSBA + 038h

Default Flash Address: 138h

Offset from 0	Bits	Description	Usage	FIT Visible
0x138h	7	Reserved, set to '0'		No
	6:4	<b>Top Swap Block size (TSBS):</b>  000 = 64 KB. Invert A16 if Top Swap is enabled 001 = 128 KB. Invert A17 if Top Swap is enabled 010 = 256 KB. Invert A18 if Top Swap is enabled 011 = 512 KB. Invert A19 if Top Swap is enabled 100 = 1 MB. Invert A20 if Top Swap is enabled 101 - 111: Reserved.  <b>Notes:</b> 1. This setting is dependent on BIOS architecture and can be different per design. The BIOS developer for the target platform has to determine this value. 2. If FWH is set as Boot BIOS destination then PCH only supports 64 KB Top Swap block size. This value has to be determined by how BIOS implements Boot-Block. 3. Intel Client chipset supports top swap block size of up to 256 KB. TS block sizes of greater than 256KB are not supported.	This allows for the system to use alternate code in order to boot a platform based upon the <b>Top Swap</b> (GPIO66/SDIO_D0 pulled low during the rising edge of <b>PWROK</b> .) strap being asserted.  <b>Top Swap</b> inverts an address on access to SPI and firmware hub, so the processor fetches the alternate Top Swap block instead of the original boot-block. The size of the Top Swap block and setting of this field must be determined by the BIOS developer. If this is not set correctly, then BIOS boot-block recovery mechanism will not work.  <b>Note:</b> This setting is not the same for all designs, is dependent on the architecture of BIOS. The setting of this field must be determined by the BIOS developer.	Yes
	3:0	Reserved, set to '0'		No

## 9.55 PCH Descriptor Record 54 (Flash Descriptor Records)

Flash Address: FPSBA + 039h

Default Flash Address: 139h

Offset from 0	Bits	Description	Usage	FIT Visible
0x139h	7:0	Reserved, set to '0'		No

## 9.56 PCH Descriptor Record 55 (Flash Descriptor Records)

Flash Address: FPSBA + 03Ah

Default Flash Address: 13Ah

Offset from 0	Bits	Description	Usage	FIT Visible
0x13Ah	7:0	Reserved, set to '0'		No





## 9.57 PCH Descriptor Record 56 (Flash Descriptor Records)

Flash Address: FPSBA + 03Bh

Default Flash Address: 13Bh

Offset from 0	Bits	Description	Usage	FIT Visible
0x13Bh	7:6	<b>SPI Maximum write and erase Resume to Suspend intervals:</b>  00 = 128us 01 = 256us 10 = 512us 11 = No Ceiling	This setting specifies the maximum value for the write and erase Resume to Suspend intervals.	Yes
	5	<b>SPI Out of Order operation Enable:</b>  0 = Out or Order operation Enabled 1 = Out of Order operation Disabled	When this setting is enabled priority operations may be issued while waiting for write / erase operations to complete on the flash device. When this setting is disabled all write / erase type operations in order.	Yes
	4	<b>SPI Suspend / Resume Enable:</b>  0 = Enable suspend / resume 1 = Disable suspend / resume	When this setting is enabled writes and erases may be suspended to allow a read to be issued on the flash device. When this setting is disabled no transaction will be allowed to the busy flash device.	Yes
	3:1	<b>SPI Resume Holdoff Delay:</b>  0x0 = 0us 0x1 = 2us 0x2 = 4us 0x3 = 6us 0x4 = 8us 0x5 = 10us 0x6 = 12us 0x7 = 14us	Specifies the time after the completion of a pri_op before the flash controller sends the resume instruction. If a new pri_op is eligible to be issued prior to the end of this delay time then the pri_op is issued and the timer is re-initialized to tRHD. 3-bit field encodes count with range 0-7. tRHD = count * 2us.	Yes
	0	Reserved, set to '0'		No



## 9.58 PCH Descriptor Record 57 (Flash Descriptor Records)

Flash Address: FPSBA + 03Ch

Default Flash Address: 13Ch

Offset from 0	Bits	Description	Usage	FIT Visible
0x13Ch	7	Reserved, set to '0'		No
	6:4	<b>Intel® Precise Touch and Stylus Controller 1 Maximum Frequency (TMF):</b>  000 = 120MHz 001 = 60MHz 010 = 48MHz 011 = Reserved 100 = 30 MHz 101 = Reserved 110 = 17 MHz 111 = Reserved  <i>Note:</i> The listed frequencies are approximate.	This field allows the OEM to set an upper limit on the frequency for Touch transactions on Intel® Precise Touch and Stylus Controller 1.  Intel® ME firmware will use the value in this field along with data from the Touch device's capability register to program the Intel® Precise Touch and Stylus Controller 1 Configuration Register.	Yes
	3:0	<b>SPI Idle to Deep Power Down Timeout:</b>  Set to '0x5'	SPI Idle to Deep Power Down Timeout Default Specifies the time in microseconds that the Flash Controller waits after all activity is idle before commanding the flash devices to Deep Powerdown, time = $2^N$ microseconds	Yes

## 9.59 PCH Descriptor Record 58 (Flash Descriptor Records)

Flash Address: FPSBA + 03Dh

Default Flash Address: 13Dh

Offset from 0	Bits	Description	Usage	FIT Visible
0x13Dh	7:3	Reserved, set to '0'	<i>Note:</i> This value will be dynamically changed to 0x1 when Intel® Precise Touch and Stylus is enabled.	No
	2:0	<b>SPI TPM Clock Frequency (STCF):</b> This field is defined with a broad range to support both SOC and PCH implementations. The listed frequencies are approximate.  000 = Reserved 001 = Reserved 010 = 48MHz 011 = Reserved 100 = 30 MHz 101 = Reserved 110 = 17 MHz 111 = reserved  <i>Notes:</i> This field identifies the serial clock frequency for TPM on SPI. This field is undefined if the TPM on SPI is disabled either by soft-strap or fuse.		Yes



## 9.60 PCH Descriptor Record 59 (Flash Descriptor Records)

Flash Address: FPSBA + 03Eh

Default Flash Address: 13Eh

Offset from 0	Bits	Description	Usage	FIT Visible
0x13Eh	7:0	Reserved, set to '0'		No

## 9.61 PCH Descriptor Record 60 (Flash Descriptor Records)

Flash Address: FPSBA + 03Fh

Default Flash Address: 13Fh

Offset from 0	Bits	Description	Usage	FIT Visible
0x13Fh	7:3	Reserved, set to '0'		No
	2:0	Reserved, set to '0x5'		No

## 9.62 PCH Descriptor Record 61 (Flash Descriptor Records)

Flash Address: FPSBA + 040h

Default Flash Address: 140h

Offset from 0	Bits	Description	Usage	FIT Visible
0x140h	31:0	Global Protected Range Default (GPRD): Set to '0'	Sets the default value of the GPR0 register in the SPI Flash Controller.	Yes

## 9.63 PCH Descriptor Record 62 (Flash Descriptor Records)

Flash Address: FPSBA + 044h

Default Flash Address: 144h

Offset from 0	Bits	Description	Usage	FIT Visible
0x144h	7:0	Reserved, set to '0'		No



## 9.64 PCH Descriptor Record 63 (Flash Descriptor Records)

Flash Address: FPSBA + 045h

Default Flash Address: 145h

Offset from 0	Bits	Description	Usage	FIT Visible
0x145h	7:1	Reserved, set to '0x1'		No
	0	eSPI / EC CRC Check Enable For Slave 0 (EC/BMC):  0 = CRC Checking enabled 1 = CRC checking disabled		Yes

## 9.65 PCH Descriptor Record 64 (Flash Descriptor Records)

Flash Address: FPSBA + 046h

Default Flash Address: 146h

Offset from 0	Bits	Description	Usage	FIT Visible
0x146h	7:3	Reserved, set to '0xB'		No
	2:0	eSPI / EC Slave Device Bus Frequency: For Slave 1 (EC/BMC): Indicates the maximum frequency of the eSPI bus that is supported by the eSPI Master and platform configuration (trace length, number of Slaves, etc.). The actual frequency of the eSPI bus will be the minimum of this field and the Slave's maximum frequency advertised in its General Capabilities register.  0x0 = 20MHz 0x1 = 24MHz 0x2 = 30 MHz 0x3 = 48MHz 0x4 = 60MHz 05x = Reserved 0x6 = Reserved 0x7 = Reserved		Yes

## 9.66 PCH Descriptor Record 65 (Flash Descriptor Records)

Flash Address: FPSBA + 047h

Default Flash Address: 147h

Offset from 0	Bits	Description	Usage	FIT Visible
0x147h	7:0	Reserved, set to '0'		No



## 9.67 PCH Descriptor Record 66 (Flash Descriptor Records)

Flash Address: FPSBA + 048h

Default Flash Address: 148h

Offset from 0	Bits	Description	Usage	FIT Visible
0x148h	7:2	Reserved, set to '0'		No
	1	eSPI / EC Slave Attached Flash Channel OOO Enable:  0 = In-Order SAF Requests 1 = Out-of-Order SAF Requests		Yes
	0	eSPI / EC Slave Attached Flash Multiple Outstanding Requests Enable:  0 = Single Outstanding SAF Request 1 = Multiple Outstanding SAF Requests		Yes

## 9.68 PCH Descriptor Record 67 (Flash Descriptor Records)

Flash Address: FPSBA + 049h

Default Flash Address: 149h

Offset from 0	Bits	Description	Usage	FIT Visible
0x149h	7:1	Reserved, set to '0'		No
	0	eSPI / EC Max Outstanding Request for Master Attached Flash Channel:  0 = Maximum of 2 outstanding requests allowed  1 = Maximum of 1 outstanding requests allowed		Yes

## 9.69 PCH Descriptor Record 68 (Flash Descriptor Records)

Flash Address: FPSBA + 04Ah

Default Flash Address: 14Ah

Offset from 0	Bits	Description	Usage	FIT Visible
0x14Ah	7	Reserved, set to '0'		No
	6	eSPI Low Frequency Debug Override:  0 = eSPI Low Frequency Debug Override Enabled 1 = eSPI Low Frequency Debug Override Disabled	When enabled this setting will divide eSPI clock frequency by 8.  <b>Note:</b> This setting should only be used for debugging purposes. Leaving this setting enable will impact eSPI performance.	Yes
	5:0	Reserved, set to '0x10'		No



## 9.70 PCH Descriptor Record 69 (Flash Descriptor Records)

Flash Address: FPSBA + 04Bh

Default Flash Address: 14Bh

Offset from 0	Bits	Description	Usage	FIT Visible
0x14Bh	7:0	Reserved, set to '0'		No

## 9.71 PCH Descriptor Record 70 (Flash Descriptor Records)

Flash Address: FPSBA + 04Ch

Default Flash Address: 14Ch

Offset from 0	Bits	Description	Usage	FIT Visible
0x14Ch	7:0	Reserved, set to '0'		No

## 9.72 PCH Descriptor Record 71 (Flash Descriptor Records)

Flash Address: FPSBA + 04Dh

Default Flash Address: 14Dh

Offset from 0	Bits	Description	Usage	FIT Visible
0x14Dh	7:5	Reserved, set to '0'		No
	4:3	<b>PCIe Controller 1 (Port 1-4):</b> Straps to set the default value of the PCI Express Port Configuration 1 register covering PCIe ports 1-4.  00 = 4x1 01 = 1x2, 2x1 10 = 2x2 11 = 1x4  <b>NOTE:</b> Refer to EDS for PCIe supported port configurations.	Setting of this field depend on what PCIe ports 1-4 configurations are desired by the board manufacturer.  <b>NOTE:</b> This field must be determined by the PCI Express port requirements of the design. The platform hardware designer must determine this setting.	Yes
	2	<b>PCIe Controller 1 Lane Reversal:</b>  0 = PCIe Lanes are not reversed. 1 = PCIe Lanes are reversed.  <b>Note:</b> Refer to EDS supported Lane reversal configuration.	This bit controls lane reversal behavior for PCIe Controller 1 for PCIe.  PCI Express port lane reversal can be done to aid in the laying out of the board.  <b>Note:</b> This setting is dependent on the board design. The platform hardware designer must determine if this port needs lane reversal.	Yes
	1:0	Reserved, set to '0'		No



## 9.73 PCH Descriptor Record 72 (Flash Descriptor Records)

Flash Address: FPSBA + 04Eh

Default Flash Address: 14Eh

Offset from 0	Bits	Description	Usage	FIT Visible
0x14Eh	7:0	Reserved, set to '0'		No

## 9.74 PCH Descriptor Record 73 (Flash Descriptor Records)

Flash Address: FPSBA + 04Fh

Default Flash Address: 14Fh

Offset from 0	Bits	Description	Usage	FIT Visible
0x14Fh	7:0	Reserved, set to '0'		No

## 9.75 PCH Descriptor Record 74 (Flash Descriptor Records)

Flash Address: FPSBA + 050h

Default Flash Address: 150h

Offset from 0	Bits	Description	Usage	FIT Visible
0x150h	7:0	Reserved, set to '0'		No

## 9.76 PCH Descriptor Record 75 (Flash Descriptor Records)

Flash Address: FPSBA + 051h

Default Flash Address: 151h

Offset from 0	Bits	Description	Usage	FIT Visible
0x151h	7:0	Reserved, set to '0'		No

## 9.77 PCH Descriptor Record 76 (Flash Descriptor Records)

Flash Address: FPSBA + 052h

Default Flash Address: 152h

Offset from 0	Bits	Description	Usage	FIT Visible
0x152h	7:0	Reserved, set to '0'		No



## 9.78 PCH Descriptor Record 77 (Flash Descriptor Records)

Flash Address: FPSBA + 053h

Default Flash Address: 153h

Offset from 0	Bits	Description	Usage	FIT Visible
0x153h	7:0	Reserved, set to '0'		No

## 9.79 PCH Descriptor Record 78 (Flash Descriptor Records)

Flash Address: FPSBA + 054h

Default Flash Address: 154h

Offset from 0	Bits	Description	Usage	FIT Visible
0x154h	7:0	Reserved, set to '0'		No

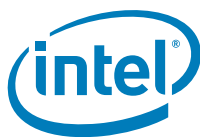
## 9.80 PCH Descriptor Record 79 (Flash Descriptor Records)

Flash Address: FPSBA + 055h

Default Flash Address: 155h

Offset from 0	Bits	Description	Usage	FIT Visible
0x155h	7:5	Reserved, set to '0'		No
	4:3	<b>PCIe Controller 2 (Port 5-8):</b>  Straps to set the default value of the PCI Express Port Configuration 1 register covering PCIe ports 5-8.  00 = 4x1 01 = 1x2, 2x1 10 = 2x2 11 = 1x4  <b>NOTE:</b> Refer to EDS for PCIe supported port configurations.	Setting of this field depend on what PCIe ports 5-8 configurations are desired by the board manufacturer.  <b>NOTE:</b> This field must be determined by the PCI Express port requirements of the design. The platform hardware designer must determine this setting.	Yes
	2	<b>PCIe Controller 2 Lane Reversal:</b>  0 = PCIe Lanes are not reversed. 1 = PCIe Lanes are reversed.  <b>Note:</b> Refer to EDS supported Lane reversal configuration.	This bit controls lane reversal behavior for PCIe Controller 2.  PCI Express port lane reversal can be done to aid in the laying out of the board.  <b>Note:</b> This setting is dependent on the board design. The platform hardware designer must determine if this port needs lane reversal.	Yes
	1:0	Reserved, set to '0'		No





## 9.81 PCH Descriptor Record 80 (Flash Descriptor Records)

Flash Address: FPSBA + 056h

Default Flash Address: 156h

Offset from 0	Bits	Description	Usage	FIT Visible
0x156h	7:0	Reserved, set to '0'		No

## 9.82 PCH Descriptor Record 81 (Flash Descriptor Records)

Flash Address: FPSBA + 057h

Default Flash Address: 157h

Offset from 0	Bits	Description	Usage	FIT Visible
0x157h	7:0	Reserved, set to '0'		No

## 9.83 PCH Descriptor Record 82 (Flash Descriptor Records)

Flash Address: FPSBA + 058h

Default Flash Address: 158h

Offset from 0	Bits	Description	Usage	FIT Visible
0x158h	7:0	Reserved, set to '0'		No

## 9.84 PCH Descriptor Record 83 (Flash Descriptor Records)

Flash Address: FPSBA + 059h

Default Flash Address: 159h

Offset from 0	Bits	Description	Usage	FIT Visible
0x159h	7:0	Reserved, set to '0'		No

## 9.85 PCH Descriptor Record 84 (Flash Descriptor Records)

Flash Address: FPSBA + 05Ah

Default Flash Address: 15Ah

Offset from 0	Bits	Description	Usage	FIT Visible
0x15Ah	7:0	Reserved, set to '0'		No



## 9.86 PCH Descriptor Record 85 (Flash Descriptor Records)

Flash Address: FPSBA + 05Bh

Default Flash Address: 15Bh

Offset from 0	Bits	Description	Usage	FIT Visible
0x15Bh	7:0	Reserved, set to '0'		No

## 9.87 PCH Descriptor Record 86 (Flash Descriptor Records)

Flash Address: FPSBA + 05Ch

Default Flash Address: 15Ch

Offset from 0	Bits	Description	Usage	FIT Visible
0x15Ch	7:0	Reserved, set to '0'		No

## 9.88 PCH Descriptor Record 87 (Flash Descriptor Records)

Flash Address: FPSBA + 05Dh

Default Flash Address: 15Dh

Offset from 0	Bits	Description	Usage	FIT Visible
0x15Dh	7:5	Reserved, set to '0'		No
	4:3	<b>PCIe Controller 3 (Port 9-12):</b> Straps to set the default value of the PCI Express Port Configuration 1 register covering PCIe ports 9-12.  00 = 4x1 01 = 1x2, 2x1 10 = 2x2 11 = 1x4  <b>NOTE:</b> Refer to EDS for PCIe supported port configurations	Setting of this field depend on what PCIe ports 9-12 configurations are desired by the board manufacturer.  <b>NOTE:</b> This field must be determined by the PCI Express port requirements of the design. The platform hardware designer must determine this setting.	Yes
	2	<b>PCIe Controller 3 Lane Reversal:</b>  This bit controls lane reversal behavior for PCIe Controller 3.  0 = PCIe Lanes are not reversed. 1 = PCIe Lanes are reversed.  <b>Note:</b> Refer to EDS supported Lane reversal configuration.	Configuring PCIe Controller 3 for PCIe Lane reversal is done via this strap.  PCI Express port lane reversal can be done to aid in the laying out of the board.  <b>Note:</b> This setting is dependent on the board design. The platform hardware designer must determine if this port needs lane reversal.	Yes
	1:0	Reserved, set to '0'		No



## 9.89 PCH Descriptor Record 88 (Flash Descriptor Records)

Flash Address: FPSBA + 05Eh

Default Flash Address: 15Eh

Offset from 0	Bits	Description	Usage	FIT Visible
0x15Eh	7:0	Reserved, set to '0'		No

## 9.90 PCH Descriptor Record 89 (Flash Descriptor Records)

Flash Address: FPSBA + 05Fh

Default Flash Address: 15Fh

Offset from 0	Bits	Description	Usage	FIT Visible
0x15Fh	7	<b>PCIe Controller 3 Port 4 SRIS:</b>  0x0 = Disabled 0x1 = Enabled	This is used to configure the platform the Intel® RST for PCIe (SATA Express) interface on <b>PCIe Controller 3 (Port 9-12)</b> .  <b>Note:</b> 1. Only 2 concurrent SATA Express devices supported for Cannonlake-LP.	Yes
	6	<b>PCIe Controller 3 Port 3 SRIS:</b>  0x0 = Disabled 0x1 = Enabled	This is used to configure the platform the Intel® RST for PCIe (SATA Express) interface on <b>PCIe Controller 3 (Port 9-12)</b> .  <b>Note:</b> 1. Only 2 concurrent SATA Express devices supported for Cannonlake-LP.	Yes
	5	<b>PCIe Controller 3 Port 2 SRIS:</b>  0x0 = Disabled 0x1 = Enabled	This is used to configure the platform the Intel® RST for PCIe (SATA Express) interface on <b>PCIe Controller 3 (Port 9-12)</b> .  <b>Note:</b> 1. Only 2 concurrent SATA Express devices supported for Cannonlake-LP.	Yes
	4	<b>PCIe Controller 3 Port 1 SRIS:</b>  0x0 = Disabled 0x1 = Enabled	This is used to configure the platform the Intel® RST for PCIe (SATA Express) interface on <b>PCIe Controller 3 (Port 9-12)</b> .  <b>Note:</b> 1. Only 2 concurrent SATA Express devices supported for Cannonlake-LP.	Yes
	3:0	Reserved, set to '0'		No

## 9.91 PCH Descriptor Record 90 (Flash Descriptor Records)

Flash Address: FPSBA + 060h

Default Flash Address: 160h

Offset from 0	Bits	Description	Usage	FIT Visible
0x160h	7:0	Reserved, set to '0'		No



## 9.92 PCH Descriptor Record 91 (Flash Descriptor Records)

Flash Address: FPSBA + 061h

Default Flash Address: 161h

Offset from 0	Bits	Description	Usage	FIT Visible
0x161h	7:0	Reserved, set to '0'		No

## 9.93 PCH Descriptor Record 92 (Flash Descriptor Records)

Flash Address: FPSBA + 062h

Default Flash Address: 162h

Offset from 0	Bits	Description	Usage	FIT Visible
0x162h	7:0	Reserved, set to '0'		No

## 9.94 PCH Descriptor Record 93 (Flash Descriptor Records)

Flash Address: FPSBA + 063h

Default Flash Address: 163h

Offset from 0	Bits	Description	Usage	FIT Visible
0x163h	7:0	Reserved, set to '0'		No

## 9.95 PCH Descriptor Record 94 (Flash Descriptor Records)

Flash Address: FPSBA + 064h

Default Flash Address: 164h

Offset from 0	Bits	Description	Usage	FIT Visible
0x164h	7:0	Reserved, set to '0'		No



## 9.96 PCH Descriptor Record 95 (Flash Descriptor Records)

Flash Address: FPSBA + 065h

Default Flash Address: 165h

Offset from 0	Bits	Description	Usage	FIT Visible
0x165h	7:5	Reserved, set to '0'		No
	4:3	<b>PCIe Controller 4 (Port 13-16):</b> Straps to set the default value of the PCI Express Port Configuration 4 register covering PCIe ports 13-16.  00 = 4x1 01 = 1x2, 2x1 10 = 2x2 11 = 1x4  <b>Note:</b> Refer to EDS for PCIe supported port configurations.	Setting of this field depend on what PCIe ports 13-16 configurations are desired by the board manufacturer.  <b>Note:</b> This field must be determined by the PCI Express port requirements of the design. The platform hardware designer must determine this setting.	Yes
	2	<b>PCIe Controller 4 Lane Reversal:</b>  0 = PCIe Lanes are not reversed. 1 = PCIe Lanes are reversed.  <b>Note:</b> Refer to EDS supported Lane reversal configuration.	This bit controls lane reversal behavior for PCIe Controller 4.  PCI Express port lane reversal can be done to aid in the laying out of the board.  <b>Note:</b> This setting is dependent on the board design. The platform hardware designer must determine if this port needs lane reversal.	Yes
	1:0	Reserved, set to '0'		No

## 9.97 PCH Descriptor Record 96 (Flash Descriptor Records)

Flash Address: FPSBA + 066h

Default Flash Address: 166h

Offset from 0	Bits	Description	Usage	FIT Visible
0x166h	7:0	Reserved, set to '0'		No



## 9.98 PCH Descriptor Record 97 (Flash Descriptor Records)

Flash Address: FPSBA + 067h

Default Flash Address: 167h

Offset from 0	Bits	Description	Usage	FIT Visible
0x167h	7	<b>PCIe Controller 4 Port 4 SRIS:</b>  0x0 = Disabled 0x1 = Enabled	This is used to configure the platform the Intel® RST for PCIe (SATA Express) interface on <b>PCIe Controller 4 (Port 13-16)</b> .  <b>Note:</b> 1. Only 2 concurrent SATA Express devices supported for Cannonlake-LP.	Yes
	6	<b>PCIe Controller 4 Port 3 SRIS:</b>  0x0 = Disabled 0x1 = Enabled	This is used to configure the platform the Intel® RST for PCIe (SATA Express) interface on <b>PCIe Controller 4 (Port 13-16)</b> .  <b>Note:</b> 1. Only 2 concurrent SATA Express devices supported for Cannonlake-LP.	Yes
	5	<b>PCIe Controller 4 Port 2 SRIS:</b>  0x0 = Disabled 0x1 = Enabled	This is used to configure the platform the Intel® RST for PCIe (SATA Express) interface on <b>PCIe Controller 4 (Port 13-16)</b> .  <b>Note:</b> 1. Only 2 concurrent SATA Express devices supported for Cannonlake-LP.	Yes
	4	<b>PCIe Controller 4 Port 1 SRIS:</b>  0x0 = Disabled 0x1 = Enabled	This is used to configure the platform the Intel® RST for PCIe (SATA Express) interface on <b>PCIe Controller 4 (Port 13-16)</b> .  <b>Note:</b> 1. Only 2 concurrent SATA Express devices supported for Cannonlake-LP.	Yes
	3:0	Reserved, set to '0'		No

## 9.99 PCH Descriptor Record 98 (Flash Descriptor Records)

Flash Address: FPSBA + 068h

Default Flash Address: 168h

Offset from 0	Bits	Description	Usage	FIT Visible
0x168h	7:0	Reserved, set to '0'		No

## 9.100 PCH Descriptor Record 99 (Flash Descriptor Records)

Flash Address: FPSBA + 069h

Default Flash Address: 169h

Offset from 0	Bits	Description	Usage	FIT Visible
0x169h	7:0	Reserved, set to '0'		No



## 9.101 PCH Descriptor Record 100 (Flash Descriptor Records)

Flash Address: FPSBA + 06Ah

Default Flash Address: 16Ah

Offset from 0	Bits	Description	Usage	FIT Visible
0x16Ah	7:0	Reserved, set to '0'		No

## 9.102 PCH Descriptor Record 101 (Flash Descriptor Records)

Flash Address: FPSBA + 06Bh

Default Flash Address: 16Bh

Offset from 0	Bits	Description	Usage	FIT Visible
0x16Bh	7:0	Reserved, set to '0'		No

## 9.103 PCH Descriptor Record 102 (Flash Descriptor Records)

Flash Address: FPSBA + 06Ch

Default Flash Address: 16Ch

Offset from 0	Bits	Description	Usage	FIT Visible
0x16Ch	7:4	Reserved, set to '0xf'		No
	3	Reserved, set to '0'		No
	2	Reserved, set to '0x1'		No
	1:0	Reserved, set to '0'		No



## 9.104 PCH Descriptor Record 103 (Flash Descriptor Records)

Flash Address: FPSBA + 06Dh

Default Flash Address: 16Dh

Offset from 0	Bits	Description	Usage	FIT Visible
0x16Dh	7	Reserved, set to '0'		No
	6:4	<b>OPI Link Width (OPDMI_LW):</b>  000 = 1 Lane 001 = 2 Lanes 010 = 4 Lanes 011 = 8 Lanes	This setting configures the OPI Link Width. For further details see the Canonlake PCH EDS.	Yes
	3:0	<b>OPI Link Speed (OPDMI_TLS):</b>  0x2 = 2 GT/s Link Speed 0x3 = 4 GT/s Link Speed	This strap must be configured when setting OPI Link Speed Strap ( <b>OPDMI_STRP</b> ).  <b>Note:</b> This strap and the OPI Link Speed Strap ( <b>OPDMI_STRP</b> ) must match the same GT configuration setting for proper platform operation function.  This setting configures the OPI Link Width. For further details see the Canonlake PCH EDS.	Yes

## 9.105 PCH Descriptor Record 104 (Flash Descriptor Records)

Flash Address: FPSBA + 06Eh

Default Flash Address: 16Eh

Offset from 0	Bits	Description	Usage	FIT Visible
0x16Eh	7	Reserved, set to '0'		No
	6	<b>DMI Lane Reversal (DMILR):</b>  0 = DMI Lanes are not reversed. 1 = DMI Lanes are reversed.	This field is used only when DMI Lanes are reversed on the layout. This usually only is done on layout constrained boards where reversing lanes help routing.  <b>Note:</b> This setting is dependent on the board design. The platform hardware designer must determine if DMI needs lane reversal.	Yes
	5	Reserved, set to '0'		No
	4:2	Reserved, set to '0x1'		No
	1:0	Reserved, set to '0'		No





## 9.106 PCH Descriptor Record 105 (Flash Descriptor Records)

Flash Address: FPSBA + 06Fh

Default Flash Address: 16Fh

Offset from 0	Bits	Description	Usage	FIT Visible
0x16Fh	7:6	Reserved, set to '0'		No
	5	Reserved, set to '0x1'		No
	3:4	Reserved, set to '0'		No
	2:1	<b>OPI Link Voltage (OPD_LVO):</b>  0 = 0.95 Volts 1 = 0.85 Volts 2 = 1.05 Volts	This strap must be configured when setting OPI Link Speed strap (OPD_LVO_STRP).  <b>Note:</b> This strap and the OPI Link Speed strap (OPD_LVO_STRP) must match the same voltage configuration setting for proper platform operation function.  This setting configures the OPI Link Voltage. For further details see Canonlake PCH EDS.	Yes
	0	Reserved, set to '0'		No

## 9.107 PCH Descriptor Record 106 (Flash Descriptor Records)

Flash Address: FPSBA + 070h

Default Flash Address: 170h

Offset from 0	Bits	Description	Usage	FIT Visible
0x170h	31	Reserved, set to '0x1'		No
	30:22	Reserved, set to '0'		No
	21	<b>Intel® Trace Hub - Emergency Mode:</b>  0 = ROM Tracing Emergency mode disabled 1 = ROM Tracing Emergency mode enabled	This option enables ROM Tracing in the base platform image.	Yes
	20	<b>Deep Sx Enable (Deep_SX_EN):</b>  0 = Deep Sx is not supported on the platform 1 = Deep Sx is supported on the platform	This requires the target platform to support Deep Sx state  <b>Note:</b> When configuring Deep Sx you must also set DEEPSX_PLT_CFG_SS.	Yes
	19	<b>SPI Software Binding Enable:</b>  0 = SPI Software Binding Disabled 1 = SPI Software Binding Enabled	When enabled this settings will allow for SPI re-binding to a new PCH during manufacturing and remanufacturing flows prior to platform EOM.  <b>Note:</b> Re-binding to a replacement PCH can only be done a maximum of 5 times before the SPI part needs to be re-flashed.	Yes
	18	Reserved, set to '0'		No
	17	<b>Direct Connect Interface (DCI) Enabled:</b>  0 = DCI Disabled 1 = DCI Enabled		Yes



Offset from 0	Bits	Description	Usage	FIT Visible
0x170h (Cont)	16	Reserved, set to '0'		Yes
	15:4	Reserved, set to '0x1b'		No
	3	<b>Intel® ME Reset Behavior:</b> 0 = Intel® ME will attempt to boot from the next available image, if it exists 1 = Intel® ME will halt	This setting determines Intel® ME behavior when boot image errors are encountered. <b>Warning:</b> This setting should be used for debug purposes only. <b>Note:</b> This may block normal firmware functional flows.	Yes
	2:1	Reserved, set to '0'		
	0	<b>Firmware ROM Bypass Enable Softstrap:</b> 0 = ROM Bypass disabled 1 = ROM Bypass enabled	Firmware ROM Bypass Enable Softstrap.	Yes

## 9.108 PCH Descriptor Record 107 (Flash Descriptor Records)

Flash Address: FPSBA + 074h

Default Flash Address: 174h

Offset from 0	Bits	Description	Usage	FIT Visible
0x174h	7:1	Reserved, set to '0'		No
	0	<b>SMBus / SMLink TCO Slave Connection:</b> 0 = TCO Slave connected to Intel® ME SMBus 1 = TCO Slave connected to Intel® ME SMBus and SMLink0	See: Cannonlake Platform Controller Hub (PCH-H) EDS for more details.	Yes

## 9.109 PCH Descriptor Record 108 (Flash Descriptor Records)

Flash Address: FPSBA + 075h

Default Flash Address: 175h

Offset from 0	Bits	Description	Usage	FIT Visible
0x175h	7:1	Reserved, set to '0'		No
	0	<b>Intel® ME SMBus Enable:</b> This bit must always be set to 1.		No



## 9.110 PCH Descriptor Record 109 (Flash Descriptor Records)

Flash Address: FPSBA + 076h

Default Flash Address: 176h

Offset from 0	Bits	Description	Usage	FIT Visible
0x176h	7:0	Reserved, set to '0'		No

## 9.111 PCH Descriptor Record 110 (Flash Descriptor Records)

Flash Address: FPSBA + 077h

Default Flash Address: 177h

Offset from 0	Bits	Description	Usage	FIT Visible
0x177h	7	Reserved, set to '0'		No
	6:0	<b>Intel® ME SMBus I<sup>2</sup>C Address (MESMI2CA):</b> Defines 7 bit Intel ME SMBus I2C target address  <b>Default set to '0'</b>  <b>Note:</b> This field is only used for testing purposes.	This address is only used by Intel® ME FW for testing purposes. If <b>MESMI2CEN</b> (Offset 0x10A bit 0) is set to 1 then the address used in this field must be non-zero and not conflict with any other devices on the segment.	Yes

## 9.112 PCH Descriptor Record 111 (Flash Descriptor Records)

Flash Address: FPSBA + 078h

Default Flash Address: 178h

Offset from 0	Bits	Description	Usage	FIT Visible
0x178h	7	Reserved, set to '0'		No
	6:0	<b>Intel® ME SMBus ASD Address (MESMASDA):</b> Intel® ME SMBus Controller ASD Target Address. ASD: Alert Sending Device  <b>Default set to '0'</b>  <b>Note:</b> This field is only applicable if there is an ASD attached to SMBus and using Intel® AMT	If <b>MESMASDEN</b> (PCH Descriptor Record 8 bit 0) is set to '1' there must be a valid address for ASD. The address must be determined by the BIOS developer based on the requirements below.  A valid address must be: <ul style="list-style-type: none"><li>• Non-zero value</li><li>• Must be a unique address on the Host SMBus segment</li><li>• Be compatible with the master on SMBus - For example, if the ASD address the master that needs write thermal information to an address "xy"h. Then this field must be set to xy"h.</li></ul>	Yes



## 9.113 PCH Descriptor Record 112 (Flash Descriptor Records)

Flash Address: FPSBA + 079h

Default Flash Address: 179h

Offset from 0	Bits	Description	Usage	FIT Visible
0x179h	7	Reserved, set to '0'		No
	6:0	<b>Intel® ME SMBus MCTP Address (MESMMCTPA):</b> Defines 7 bit Intel ME SMBus MCTP target address  <b>Default set to '0'</b>  <b>Note:</b> This field is only used for testing purposes.	If MESMMCTPAEN (PCHSTRP3 bit 8) is set to 1 then the address used in this field must be non-zero and not conflict with any other devices on the segment.	Yes

## 9.114 PCH Descriptor Record 113 (Flash Descriptor Records)

Flash Address: FPSBA + 07Ah

Default Flash Address: 17Ah

Offset from 0	Bits	Description	Usage	FIT Visible
0x17Ah	7:1	Reserved, set to '0'		No
0x17Ah (Cont)	0	<b>Intel® ME SMBus I<sup>2</sup>C Address Enable (MESMI2CEN):</b>  0 = Intel® ME SMBus I <sup>2</sup> C Address is disabled 1 = Intel® ME SMBus I <sup>2</sup> C Address is enabled  <b>Note:</b> This field is only used for testing purposes.	This field should only be set to '1' for testing purposes	Yes

## 9.115 PCH Descriptor Record 114 (Flash Descriptor Records)

Flash Address: FPSBA + 07Bh

Default Flash Address: 17Bh

Offset from 0	Bits	Description	Usage	FIT Visible
0x17Bh	7:1	Reserved, set to '0'		No
	0	<b>Intel® ME SMBus ASD Address Enable (MESMASDEN):</b>  0 = Intel® ME SMBus ASD Address is disabled 1 = Intel® ME SMBus ASD Address is enabled  <b>Note:</b> This field is only applicable if there is an ASD attached to SMBus and using Intel® AMT	This bit must only be set to '1' when there is an ASD (Alert Sending Device) attached to Host SMBus. This is only applicable in platforms using Intel® AMT.  <b>Note:</b> This setting is not the same for all designs, is dependent on the board design. The setting of this field must be determined by the BIOS developer and the platform hardware designer.	Yes



## 9.116 PCH Descriptor Record 115 (Flash Descriptor Records)

Flash Address: FPSBA + 07Ch

Default Flash Address: 17Ch

Offset from 0	Bits	Description	Usage	FIT Visible
0x17Ch	7:1	Reserved, set to '0'		No
	0	<b>Intel® ME SMBus MCTP Address Enable (MESMMCTPA):</b>  0 = Intel ME SMBus MCTP Address is disabled 1 = Intel ME SMBus MCTP Address is enabled  <b>Note:</b> This field is only used for testing purposes.		Yes

## 9.117 PCH Descriptor Record 116 (Flash Descriptor Records)

Flash Address: FPSBA + 07Dh

Default Flash Address: 17Dh

Offset from 0	Bits	Description	Usage	FIT Visible
0x17Dh	7:0	Reserved, set to '0'		No

## 9.118 PCH Descriptor Record 117 (Flash Descriptor Records)

Flash Address: FPSBA + 07Eh

Default Flash Address: 17Eh

Offset from 0	Bits	Description	Usage	FIT Visible
0x17Eh	31:0	<b>Intel® ME SMBus Subsystem Device ID for ASF (MESMA2UDID):</b> MESMAUDID[15:0] - Subsystem Vendor ID MESMAUDID[31:16] - Subsystem Device ID  The values contained in MESMAUDID[15:0] and MESMAUDID[31:16] are provided as bytes 8-9 and 10-11 of the data payload to an external master when it initiates a Directed GET UDID Block Read Command to the Alert Sending Device ASD's address.  Default set to '0'	This bit must only be set to '1' when there is an ASD (Alert Sending Device) attached to SMBus and when MESMASDEN (FPSBA + 0x173h) is set to '1'. This is only applicable in platforms using Intel® AMT. Set this if you want to add a 4 byte payload to an external master when a GET UDID Block read command is made to Intel ME SMBus ASD's address.	Yes



## 9.119 PCH Descriptor Record 118 (Flash Descriptor Records)

Flash Address: FPSBA + 082h

Default Flash Address: 182h

Offset from 0	Bits	Description	Usage	FIT Visible
0x182h	31:0	Reserved, set to '0'		No

## 9.120 PCH Descriptor Record 119 (Flash Descriptor Records)

Flash Address: FPSBA + 086h

Default Flash Address: 186h

Offset from 0	Bits	Description	Usage	FIT Visible
0x186h	7:2	Reserved, set to '0'		No
	1:0	<b>Intel® ME SMBus Frequency (SMB0FRO):</b> The value of these bits determine the physical bus speed supported by the HW. Set to '0x1'	Intel® ME SMBus	No

## 9.121 PCH Descriptor Record 120 (Flash Descriptor Records)

Flash Address: FPSBA + 088h

Default Flash Address: 188h

Offset from 0	Bits	Description	Usage	FIT Visible
0x188h	7:0	Reserved, set to '0x1'		No



## 9.122 PCH Descriptor Record 121 (Flash Descriptor Records)

Flash Address: FPSBA + 089h

Default Flash Address: 189h

Offset from 0	Bits	Description	Usage	FIT Visible
0x189h	7:1	Reserved, set to '0'		No
	0	<b>SMLink0 Enable (SML0_EN):</b> Configures if SMLink0 segment is enabled  0 = Disabled 1 = Enabled  <b>Notes:</b> 1. This bit MUST be set to '1' when utilizing integrated LAN controller. 2. The SMBus TCO Slave controller must be routed to this SMLink 0 Segment. 3. This segment should be set to 0 in one of the following cases: a. Disabled by the user.	The Intel PHY SMBus controller must be routed to this SMLink 0 Segment.  <b>Note:</b> This setting is not the same for all designs, is dependent on the board design. The setting of this field must be determined by the BIOS developer and the platform hardware designer.	Yes

## 9.123 PCH Descriptor Record 122 (Flash Descriptor Records)

Flash Address: FPSBA + 08Ah

Default Flash Address: 18Ah

Offset from 0	Bits	Description	Usage	FIT Visible
0x18Ah	7:0	Reserved, set to '0'		No

## 9.124 PCH Descriptor Record 123 (Flash Descriptor Records)

Flash Address: FPSBA + 08Bh

Default Flash Address: 18Bh

Offset from 0	Bits	Description	Usage	FIT Visible
0x18Bh	7:0	Reserved, set to '0'		No

## 9.125 PCH Descriptor Record 124 (Flash Descriptor Records)

Flash Address: FPSBA + 08Ch

Default Flash Address: 18Ch

Offset from 0	Bits	Description	Usage	FIT Visible
0x18Ch	7:0	Reserved, set to '0'		No



## 9.126 PCH Descriptor Record 125 (Flash Descriptor Records)

Flash Address: FPSBA + 08Dh

Default Flash Address: 18Dh

Offset from 0	Bits	Description	Usage	FIT Visible
0x18Dh	7:0	Reserved, set to '0'		No

## 9.127 PCH Descriptor Record 126 (Flash Descriptor Records)

Flash Address: FPSBA + 08Eh

Default Flash Address: 18Eh

Offset from 0	Bits	Description	Usage	FIT Visible
0x18Eh	7:0	Reserved, set to '0'		No

## 9.128 PCH Descriptor Record 127 (Flash Descriptor Records)

Flash Address: FPSBA + 08Fh

Default Flash Address: 18Fh

Offset from 0	Bits	Description	Usage	FIT Visible
0x18Fh	7:0	Reserved, set to '0'		No

## 9.129 PCH Descriptor Record 128 (Flash Descriptor Records)

Flash Address: FPSBA + 090h

Default Flash Address: 190h

Offset from 0	Bits	Description	Usage	FIT Visible
0x190h	7:0	Reserved, set to '0'		No

## 9.130 PCH Descriptor Record 129 (Flash Descriptor Records)

Flash Address: FPSBA + 091h

Default Flash Address: 191h

Offset from 0	Bits	Description	Usage	FIT Visible
0x191h	7:0	Reserved, set to '0'		No





### 9.131 PCH Descriptor Record 130 (Flash Descriptor Records)

Flash Address: FPSBA + 092h

Default Flash Address: 192h

Offset from 0	Bits	Description	Usage	FIT Visible
0x192h	31:0	Reserved, set to '0'		No

### 9.132 PCH Descriptor Record 131 (Flash Descriptor Records)

Flash Address: FPSBA + 096h

Default Flash Address: 196h

Offset from 0	Bits	Description	Usage	FIT Visible
0x196h	31:0	Reserved, set to '0'		No

### 9.133 PCH Descriptor Record 132 (Flash Descriptor Records)

Flash Address: FPSBA + 09Ah

Default Flash Address: 19Ah

Offset from 0	Bits	Description	Usage	FIT Visible
0x19Ah	7:2	Reserved, set to '0'		No
	1:0	<b>SMLink0 Frequency (SML0FRQ):</b> These bits determine the physical bus speed supported by the HW.  00 = Reserved 01 = Standard Mode - up to 100 kHz 10 = Fast Mode - up to 400 kHz 11 = Fast Mode Plus - up to 1 MHz	Speed is dependent on board topology and layout.	Yes

### 9.134 PCH Descriptor Record 133 (Flash Descriptor Records)

Flash Address: FPSBA + 09Ch

Default Flash Address: 19Ch

Offset from 0	Bits	Description	Usage	FIT Visible
0x19Ch	7:0	Reserved, set to '0x1'		No



## 9.135 PCH Descriptor Record 134 (Flash Descriptor Records)

Flash Address: FPSBA + 09Dh

Default Flash Address: 19Dh

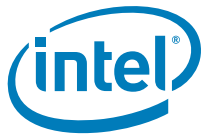
Offset from 0	Bits	Description	Usage	FIT Visible
0x19Dh	7:1	Reserved, set to '0'		No
	0	<b>SMLink1 Enable (SML1_EN):</b> Configures if SMLink1 segment is enabled  0 = Disabled 1 = Enabled  <b>Note:</b> This must be set to '1' platforms that use PCH SMBus based thermal reporting.	This bit must be set to '1' if using the PCH's Thermal reporting. If setting this bit to '0', there must be an external solution that gathers temperature information from PCH and processor.  <b>Note:</b> This setting is not the same for all designs, is dependent on the board design. The setting of this field must be determined by the BIOS developer and the platform hardware designer.	Yes

## 9.136 PCH Descriptor Record 135 (Flash Descriptor Records)

Flash Address: FPSBA + 09Eh

Default Flash Address: 19Eh

Offset from 0	Bits	Description	Usage	FIT Visible
0x19Eh	7:1	<b>SMLink1 GP Target Address (SML1GPA):</b> SMLink1 controller General Purpose Target Address (7:1)  <b>Notes:</b> 1. This field is not active unless SML1GPAEN is set to '1'. 2. This address MUST be set if there is a device on the SMLink1 segment that will use SMBus based PCH thermal reporting. 3. If SML1GPAEN = '1' then this field must be a valid 7 bit, non-zero address that does not conflict with any other devices on SMLink1 segment.  Default set to '0'	When <b>SML1GPAEN</b> = '1', there needs to be a valid GP address in this field. This address used here is design specific. The BIOS developer and / or platform hardware designer must supply an address with the criteria below.  A valid address must be: <ul style="list-style-type: none"> <li>• Non-zero value</li> <li>• Must be a unique address on the SMLink1 segment</li> <li>• Be compatible with the master on SMLink1 - For example if the GP address the master that needs read thermal information from a certain address, then this field must be set accordingly.</li> </ul>	Yes
	0	<b>SMLink1 GP Target Address Enable (SML1GPAEN):</b>  SMLink1 controller General Purpose Target Address Enable  0 = SMLink1 GP Address is disabled 1 = SMLink1 GP Address is enabled  This bit MUST set to '1' if there is a device on the SMLink1 segment that will use SMBus based PCH thermal reporting. This bit MUST be set to '0' if PCH thermal reporting is not used.	This bit must be set in cases where SMLink1 has a master that requires SMBus based Thermal Reporting that is supplied by the PCH. Some examples of this master could be an Embedded Controller, a BMC, or any other SMBus Capable device that needs Processor or PCH temperature information. If no master on the SMLink1 segment is capable of utilizing thermal reporting, then this field must be set to '0'.  <b>Note:</b> This setting is not the same for all designs, is dependent on the board design. The setting of this field must be determined by the BIOS developer and the platform hardware designer.	Yes



## 9.137 PCH Descriptor Record 136 (Flash Descriptor Records)

Flash Address: FPSBA + 09Fh

Default Flash Address: 19Fh

Offset from 0	Bits	Description	Usage	FIT Visible
0x19Fh	7	Reserved, set to '0'		No
	6:0	<b>SMLink1 I<sup>2</sup>C* Target Address (SML1I2CA):</b>  <b>Notes:</b> 1. This field is not active unless SML1I2CAEN is set to '1'. 2. This address can be different for every design, ensure BIOS developer supplies the address.  <b>Default set to '0'</b>	When <b>SML1I2CAEN</b> (PCHSTRP11 bit 24) = '1', there needs to be a valid I2C address in this field. This address used here is design specific. The BIOS developer and/or platform hardware designer must supply an address with the criteria below.  <b>A valid address must be:</b> <ul style="list-style-type: none"><li>Non-zero value</li><li>Must be a unique address on the SMLink1 segment</li></ul>	Yes

## 9.138 PCH Descriptor Record 137 (Flash Descriptor Records)

Flash Address: FPSBA + 0A0h

Default Flash Address: 1A0h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1A0h	7:0	Reserved, set to '0'		No

## 9.139 PCH Descriptor Record 138 (Flash Descriptor Records)

Flash Address: FPSBA + 0A1h

Default Flash Address: 1A1h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1A1h	7:0	Reserved, set to '0'		No

## 9.140 PCH Descriptor Record 139 (Flash Descriptor Records)

Flash Address: FPSBA + 0A2h

Default Flash Address: 1A2h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1A2h	7:1	Reserved, set to '0'		No



Offset from 0	Bits	Description	Usage	FIT Visible
0x1A2h (Cont)	0	SMLink1 I <sup>2</sup> C Target Address Enable (SML1I2CAEN): 0 = SMLink1 I <sup>2</sup> C Address is disabled 1 = SMLink1 I <sup>2</sup> C Address is enabled		Yes

## 9.141 PCH Descriptor Record 140 (Flash Descriptor Records)

Flash Address: FPSBA + 0A3h

Default Flash Address: 1A3h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1A3h	7:0	Reserved, set to '0'		No

## 9.142 PCH Descriptor Record 141 (Flash Descriptor Records)

Flash Address: FPSBA + 0A4h

Default Flash Address: 1A4h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1A4h	7:0	Reserved, set to '0'		No

## 9.143 PCH Descriptor Record 142 (Flash Descriptor Records)

Flash Address: FPSBA + 0A5h

Default Flash Address: 1A5h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1A5h	7:0	Reserved, set to '0'		No

## 9.144 PCH Descriptor Record 143 (Flash Descriptor Records)

Flash Address: FPSBA + 0A6h

Default Flash Address: 1A6h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1A6h	31:0	Reserved, set to '0'		No



## 9.145 PCH Descriptor Record 144 (Flash Descriptor Records)

Flash Address: FPSBA + 0AAh

Default Flash Address: 1AAh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1AAh	31:0	Reserved, set to '0'		No

## 9.146 PCH Descriptor Record 145 (Flash Descriptor Records)

Flash Address: FPSBA + 0AEh

Default Flash Address: 1AEh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1AEh	7:2	Reserved, set to '0'		No
	1:0	SMLink1 Frequency (SML1FRQ): 00 = Reserved 01 = Standard Mode - up to 100 kHz 10 = Fast Mode - up to 400 kHz 11 = Fast Mode Plus - up to 1 MHz		Yes

## 9.147 PCH Descriptor Record 146 (Flash Descriptor Records)

Flash Address: FPSBA + 0AFh

Default Flash Address: 1AFh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1AFh	7:0	Reserved, set to '0'		No

## 9.148 PCH Descriptor Record 147 (Flash Descriptor Records)

Flash Address: FPSBA + 0B0h

Default Flash Address: 1B0h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1B0h	7:0	Reserved, set to '0x7'		No



## 9.149 PCH Descriptor Record 148 (Flash Descriptor Records)

Flash Address: FPSBA + 0B1h

Default Flash Address: 1B1h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1B1h	7:0	Reserved, set to '0'		No

## 9.150 PCH Descriptor Record 149 (Flash Descriptor Records)

Flash Address: FPSBA + 0B2h

Default Flash Address: 1B2h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1B2h	7:0	Reserved, set to '0'		No

## 9.151 PCH Descriptor Record 150 (Flash Descriptor Records)

Flash Address: FPSBA + 0B3h

Default Flash Address: 1B3h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1B3h	7:0	Reserved, set to '0'		No

## 9.152 PCH Descriptor Record 151 (Flash Descriptor Records)

Flash Address: FPSBA + 0B4h

Default Flash Address: 1B4h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1B4h	7	Reserved, set to '0'		No
	6:0	<b>GbE MAC SMBus Address:</b> This is the 7 bit SMBus address to accept SMBus cycles from the PHY.  <b>Notes:</b> This field must be programmed to 70h.	This is the Intel integrated wired MAC's SMBus address. This field must be programmed to 70h.  GbE PHY SMBus Address and GbE MAC address have to be programmed to 64h and 70h in order to ensure proper arbitration of SMBus communication between the Intel integrated MAC and PHY.	Yes



### 9.153 PCH Descriptor Record 152 (Flash Descriptor Records)

Flash Address: FPSBA + 0B5h

Default Flash Address: 1B5h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1B5h	7:0	Reserved, set to '0'		No

### 9.154 PCH Descriptor Record 153 (Flash Descriptor Records)

Flash Address: FPSBA + 0B6h

Default Flash Address: 1B6h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1B6h	7:0	Reserved, set to '0'		No

### 9.155 PCH Descriptor Record 154 (Flash Descriptor Records)

Flash Address: FPSBA + 0B7h

Default Flash Address: 1B7h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1B7h	7:1	Reserved, set to '0'		No
	0	<b>Gbe MAC SMBus Address Enable (GBEMAC_SMBUS_ADDR_EN):</b>  0 = Disabled 1 = Enabled  <b>Notes:</b> 1. This bit MUST be set to '1' when utilizing Intel integrated wired LAN. 2. If not using Intel integrated wired LAN solution or if disabling it, then this segment must be set to '0'.	This bit must be set to '1' if Intel integrated wired LAN solution is used. If not using, or if disabling Intel integrated wired LAN solution, then this field must be set to '0'.	Yes

### 9.156 PCH Descriptor Record 155 (Flash Descriptor Records)

Flash Address: FPSBA + 0B8h

Default Flash Address: 1B8h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1B8h	7:0	Reserved, set to '0x3'		No



## 9.157 PCH Descriptor Record 156 (Flash Descriptor Records)

Flash Address: FPSBA + 0B9h

Default Flash Address: 1B9h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1B9h	7:0	Reserved, set to '0x2'		No

## 9.158 PCH Descriptor Record 157 (Flash Descriptor Records)

Flash Address: FPSBA + 0BAh

Default Flash Address: 1BAh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1BAh	7:0	Reserved, set to '0'		No

## 9.159 PCH Descriptor Record 158 (Flash Descriptor Records)

Flash Address: FPSBA + 0BBh

Default Flash Address: 1BBh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1BBh	7:0	Reserved, set to '0'		No

## 9.160 PCH Descriptor Record 159 (Flash Descriptor Records)

Flash Address: FPSBA + 0BCh

Default Flash Address: 1BCh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1BCh	7	Reserved, set to '0'		No
	6:0	<b>GbE PHY SMBus Address:</b> This is the 7 bit SMBus address the PHY uses to accept SMBus cycles from the MAC.  This field must be programmed to <b>64h</b> .	This is the Intel PHY's SMBus address. This field must be programmed to 64h.  GbE PHY SMBus Address and GbE MAC address have to be programmed to 64h and 70h in order to ensure proper arbitration of SMBus communication between the Intel integrated MAC and PHY.	Yes





## 9.161 PCH Descriptor Record 160 (Flash Descriptor Records)

Flash Address: FPSBA + 0BDh

Default Flash Address: 1BDh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1BDh	7:0	Reserved, set to '0'		No

## 9.162 PCH Descriptor Record 161 (Flash Descriptor Records)

Flash Address: FPSBA + 0BEh

Default Flash Address: 1BEh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1BEh	7:0	Reserved, set to '0'		No

## 9.163 PCH Descriptor Record 162 (Flash Descriptor Records)

Flash Address: FPSBA + 0BFh

Default Flash Address: 1BFh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1BFh	7:0	Reserved, set to '0'		No

## 9.164 PCH Descriptor Record 163 (Flash Descriptor Records)

Flash Address: FPSBA + 0C0h

Default Flash Address: 1C0h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1C0h	7:0	Reserved, set to '0'		No

## 9.165 PCH Descriptor Record 164 (Flash Descriptor Records)

Flash Address: FPSBA + 0C1h

Default Flash Address: 1C1h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1C1h	7:0	Reserved, set to '0'		No



## 9.166 PCH Descriptor Record 165 (Flash Descriptor Records)

Flash Address: FPSBA + 0C2h

Default Flash Address: 1C2h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1C2h	7:0	Reserved, set to '0'		No

## 9.167 PCH Descriptor Record 166 (Flash Descriptor Records)

Flash Address: FPSBA + 0C3h

Default Flash Address: 1C3h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1C3h	7:0	Reserved, set to '0'		No

## 9.168 PCH Descriptor Record 167 (Flash Descriptor Records)

Flash Address: FPSBA + 0C4h

Default Flash Address: 1C4h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1C4h	7:6	Reserved, set to '0'		No
	5:4	<b>Intel® RST for PCIe-C3 Select x2 or x4:</b>  00 = Reserved 01 = Intel® RST for PCIe-C3 configured for x2 10 = Intel® RST for PCIe-C3 configured for x4 11 = Reserved	This is used to configure the platform for the Intel® RST for PCIe interface to either x2 or x4 lane operation on <b>PCIe Controller 4 (Port 13-16)</b> .  <b>Note:</b> 1. Only 2 concurrent SATA Express devices supported for Cannonlake-LP.	Yes
	3:2	<b>Intel® RST for PCIe-C2 Select x2 or x4:</b>  00 = Reserved 01 = Intel® RST for PCIe-C2 configured for x2 10 = Intel® RST for PCIe-C2 configured for x4 11 = Reserved	This is used to configure the platform for the Intel® RST for PCIe interface to either x2 or x4 lane operation on <b>PCIe Controller 3 (Port 9-12)</b> .  <b>Note:</b> 1. Only 2 concurrent SATA Express devices supported for Cannonlake-LP.	Yes
	1:0	Reserved, set to '0x2'		No



## 9.169 PCH Descriptor Record 168 (Flash Descriptor Records)

Flash Address: FPSBA + 0C5h

Default Flash Address: 1C5h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1C5h	7:6	Reserved, set to '0'		No
	5:4	Intel® RST for PCIe Ctrl 3 Strap: 00 = Reserved 01 = 1x2, 2x1 10 = 2x2 11 = 1x4	This is used to configure the platform for the Intel® RST for PCIe interface to either x2 or x4 lane operation on <b>PCIe Controller 4 (Port 13-16)</b> .  <b>Note:</b> 1. Only 2 concurrent SATA Express devices supported for Cannonlake-LP. 2. When enabling the Intel® RST for PCIe interface this setting must match the port configuration <b>PCIe Controller 4 (Port 13-16)</b> and Intel® RST for PCIe Controller 4.	No
	3:2	Intel® RST for PCIe Ctrl 2 Strap: 00 = Reserved 01 = 1x2, 2x1 10 = 2x2 11 = 1x4	This is used to configure the platform for the Intel® RST for PCIe interface to either x2 or x4 lane operation on <b>PCIe Controller 3 (Port 9-12)</b> .  <b>Note:</b> 1. Only 2 concurrent SATA Express devices supported for Cannonlake-LP. 2. When enabling the Intel® RST for PCIe interface this setting must match the port configuration <b>PCIe Controller 3 (Port 9-12)</b> and Intel® RST for PCIe Controller 3.	No
	1:0	Reserved, set to '0x1'		No

## 9.170 PCH Descriptor Record 169 (Flash Descriptor Records)

Flash Address: FPSBA + 0C8h

Default Flash Address: 1C8h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1C8h	7:0	Reserved, set to '0xD'		No

## 9.171 PCH Descriptor Record 170 (Flash Descriptor Records)

Flash Address: FPSBA + 0C9h

Default Flash Address: 1C9h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1C9h	7:0	Reserved, set to '0'		No



## 9.172 PCH Descriptor Record 171 (Flash Descriptor Records)

Flash Address: FPSBA + 0CAh

Default Flash Address: 1CAh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1CAh	7:0	Reserved, set to '0'		No

## 9.173 PCH Descriptor Record 172 (Flash Descriptor Records)

Flash Address: FPSBA + 0CBh

Default Flash Address: 1CBh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1CBh	7:0	Reserved, set to '0'		No

## 9.174 PCH Descriptor Record 173 (Flash Descriptor Records)

Flash Address: FPSBA + 0CCh

Default Flash Address: 1CCh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1CCh	7:6	Reserved, set to '0'		No
	3:2	<b>Intel® RST for PCIe Controller 2:</b> 00 = Reserved 01 = 1x2, 2x1 10 = 2x2 11 = 1x4	This is used to configure the platform for the Intel® RST for PCIe interface to either x2 or x4 lane operation on <b>PCIe Controller 3 (Port 9-12)</b> .  <b>Note:</b> 1. Only 2 concurrent SATA Express devices supported for Cannonlake-LP. 2. When enabling the Intel® RST for PCIe interface this setting must match the port configuration <b>PCIe Controller 3 (Port 9-12)</b> and Intel® RST for PCIe Ctrl 3 Strap.	Yes
	1:0	Reserved, set to '0x1'		No

## 9.175 PCH Descriptor Record 174 (Flash Descriptor Records)

Flash Address: FPSBA + 0CDh

Default Flash Address: 1CDh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1CDh	7:0	Reserved, set to '0'		No



## 9.176 PCH Descriptor Record 175 (Flash Descriptor Records)

Flash Address: FPSBA + 0CEh

Default Flash Address: 1CEh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1CEh	7:0	Reserved, set to '0'		No

## 9.177 PCH Descriptor Record 176 (Flash Descriptor Records)

Flash Address: FPSBA + 0CFh

Default Flash Address: 1CFh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1CFh	7:0	Reserved, set to '0'		No

## 9.178 PCH Descriptor Record 177 (Flash Descriptor Records)

Flash Address: FPSBA + 0D0h

Default Flash Address: 1D0h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1D0h	7:6	Reserved, set to '0'		No
	5:4	Intel® RST for PCIe Controller 3: 00 = Reserved 01 = 1x2, 2x1 10 = 2x2 11 = 1x4	This is used to configure the platform for the Intel® RST for PCIe interface to either x2 or x4 lane operation on PCIe Controller 4 (Port 13-16).  <b>Note:</b> 1. Only 2 concurrent SATA Express devices supported for Cannonlake-LP. 2. When enabling the Intel® RST for PCIe interface this setting must match the port configuration PCIe Controller 4 (Port 13-16) and Intel® RST for PCIe Ctrl 4 Strap.	Yes
	3:2	Reserved, set to '0x3'		No
	1:0	Reserved, set to '0x1'		No

## 9.179 PCH Descriptor Record 178 (Flash Descriptor Records)

Flash Address: FPSBA + 0D4h

Default Flash Address: 1D4h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1D4h	7:0	Reserved, set to '0'		No



## 9.180 PCH Descriptor Record 179 (Flash Descriptor Records)

Flash Address: FPSBA + 0D5h

Default Flash Address: 1D5h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1D5h	7:0	Reserved, set to '0'		No

## 9.181 PCH Descriptor Record 180 (Flash Descriptor Records)

Flash Address: FPSBA + 0D6h

Default Flash Address: 1D6h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1D6h	7:0	Reserved, set to '0'		No

## 9.182 PCH Descriptor Record 181 (Flash Descriptor Records)

Flash Address: FPSBA + 0D7h

Default Flash Address: 1D7h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1D7h	7:0	Reserved, set to '0'		No

## 9.183 PCH Descriptor Record 182 (Flash Descriptor Records)

Flash Address: FPSBA + 0D8h

Default Flash Address: 1D8h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1D8h	7:0	Reserved, set to '0'		No

## 9.184 PCH Descriptor Record 183 (Flash Descriptor Records)

Flash Address: FPSBA + 0D9h

Default Flash Address: 1D9h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1D9h	7:0	Reserved, set to '0'		No



## 9.185 PCH Descriptor Record 184 (Flash Descriptor Records)

Flash Address: FPSBA + 0DAh

Default Flash Address: 1DAh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1DAh	7:0	Reserved, set to '0'		No

## 9.186 PCH Descriptor Record 185 (Flash Descriptor Records)

Flash Address: FPSBA + 0DBh

Default Flash Address: 1DBh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1DBh	7:0	Reserved, set to '0'		No

## 9.187 PCH Descriptor Record 186 (Flash Descriptor Records)

Flash Address: FPSBA + 0DCh

Default Flash Address: 1DCh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1DCh	7:0	Reserved, set to '0'		No

## 9.188 PCH Descriptor Record 187 (Flash Descriptor Records)

Flash Address: FPSBA + 0DDh

Default Flash Address: 1DDh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1DDh	7:0	Reserved, set to '0'		No

## 9.189 PCH Descriptor Record 188 (Flash Descriptor Records)

Flash Address: FPSBA + 0DEh

Default Flash Address: 1DEh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1DEh	7:0	Reserved, set to '0'		No



## 9.190 PCH Descriptor Record 189 (Flash Descriptor Records)

Flash Address: FPSBA + 0DFh

Default Flash Address: 1DFh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1DFh	7:0	Reserved, set to '0'		No

## 9.191 PCH Descriptor Record 190 (Flash Descriptor Records)

Flash Address: FPSBA + 0E0h

Default Flash Address: 1E0h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1E0h	7:0	Reserved, set to '0'		No

## 9.192 PCH Descriptor Record 191 (Flash Descriptor Records)

Flash Address: FPSBA + 0E1h

Default Flash Address: 1E1h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1E1h	7:0	Reserved, set to '0'		No

## 9.193 PCH Descriptor Record 192 (Flash Descriptor Records)

Flash Address: FPSBA + 0E2h

Default Flash Address: 1E2h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1E2h	7:0	Reserved, set to '0'		No

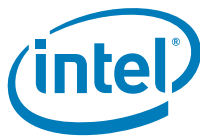
## 9.194 PCH Descriptor Record 193 (Flash Descriptor Records)

Flash Address: FPSBA + 0E3h

Default Flash Address: 1E3h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1E3h	7:0	Reserved, set to '0'		No





## 9.195 PCH Descriptor Record 194 (Flash Descriptor Records)

Flash Address: FPSBA + 0E4h

Default Flash Address: 1E4h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1E4h	7	<b>DCI BSSB over USB3 Port5 Configuration (EXI_PTSS_PORT7):</b>  0 = BSSB is enabled on USB3 Port5 1 = BSSB is disabled on USB3 Port5	This setting determines if the USB port being used for <b>DCI</b> operations has BSSB (Boundary Scan Side Band) enabled.  <b>Note:</b> For S0ix and reset flows BSSB should be enabled.	Yes
	6	<b>DCI BSSB over USB3 Port4 Configuration (EXI_PTSS_PORT6):</b>  0 = BSSB is enabled on USB3 Port4 1 = BSSB is disabled on USB3 Port4	This setting determines if the USB port being used for <b>DCI</b> operations has BSSB (Boundary Scan Side Band) enabled.  <b>Note:</b> For S0ix and reset flows BSSB should be enabled.	Yes
	5	<b>DCI BSSB over USB3 Port3 Configuration (EXI_PTSS_PORT5):</b>  0 = BSSB is enabled on USB3 Port3 1 = BSSB is disabled on USB3 Port3	This setting determines if the USB port being used for <b>DCI</b> operations has BSSB (Boundary Scan Side Band) enabled.  <b>Note:</b> For S0ix and reset flows BSSB should be enabled.	Yes
	4	<b>DCI BSSB over USB3 Port2 Configuration (EXI_PTSS_PORT4):</b>  0 = BSSB is enabled on USB3 Port2 1 = BSSB is disabled on USB3 Port2	This setting determines if the USB port being used for <b>DCI</b> operations has BSSB (Boundary Scan Side Band) enabled.  <b>Note:</b> For S0ix and reset flows BSSB should be enabled.	Yes
	3	Reserved, set to '0'		No
	2	<b>DCI BSSB over GPIO Configuration (EXI_PTSS_PORT2):</b>  0 = BSSB is enabled over GPIO 1 = BSSB is disabled over GPIO	This setting enables BSSB (Boundary Scan Side Band) over GPIO for <b>DCI</b> operations.  <b>Note:</b> If this setting is enabled the <b>DCI Port1 Configuration</b> also needs to be enabled. <b>Note:</b> For S0ix and reset flows BSSB should be enabled.	Yes
	1	Reserved, set to '0'		No
	0	<b>DCI BSSB over USB3 Port1 Configuration (EXI_PTSS_PORT0):</b>  0 = BSSB is enabled on USB3 Port1 1 = BSSB is disabled on USB3 Port1	This setting determines if the USB port being used for <b>DCI</b> operations has BSSB (Boundary Scan Side Band) enabled.  <b>Note:</b> For S0ix and reset flows BSSB should be enabled.	Yes



## 9.196 PCH Descriptor Record 195 (Flash Descriptor Records)

Flash Address: FPSBA + 0E5h

Default Flash Address: 1E5h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1E5h	7:1	Reserved, set to '0x7f'		No
	0	<b>DCI BSSB over USB3 Port6 Configuration (EXI_PTSS_PORT8):</b> 0 = BSSB is enabled on USB3 Port6 1 = BSSB is disabled on USB3 Port6	This setting determines if the USB port being used for <b>DCI</b> operations has BSSB (Boundary Scan Side Band) enabled.  <b>Note:</b> For S0ix and reset flows BSSB should be enabled.	Yes

## 9.197 PCH Descriptor Record 196 (Flash Descriptor Records)

Flash Address: FPSBA + 0E6h

Default Flash Address: 1E6h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1E6h	7:0	Reserved, set to '0'		No

## 9.198 PCH Descriptor Record 197 (Flash Descriptor Records)

Flash Address: FPSBA + 0E7h

Default Flash Address: 1E7h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1E7h	7:0	Reserved, set to '0'		No

## 9.199 PCH Descriptor Record 198 (Flash Descriptor Records)

Flash Address: FPSBA + 0E8h

Default Flash Address: 1E8h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1E8h	7:0	Reserved, set to '0'		No



## 9.200 PCH Descriptor Record 199 (Flash Descriptor Records)

Flash Address: FPSBA + 0E9h

Default Flash Address: 1E9h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1E9h	7:0	Reserved, set to '0'		No

## 9.201 PCH Descriptor Record 200 (Flash Descriptor Records)

Flash Address: FPSBA + 0EAh

Default Flash Address: 1EAh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1EAh	7:0	Reserved, set to '0x7'		No

## 9.202 PCH Descriptor Record 201 (Flash Descriptor Records)

Flash Address: FPSBA + 0EBh

Default Flash Address: 1EBh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1EBh	7:0	Reserved, set to '0x68'		No

## 9.203 PCH Descriptor Record 202 (Flash Descriptor Records)

Flash Address: FPSBA + 0ECh

Default Flash Address: 1ECh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1ECh	7:4	Reserved, set to '0'		No
	3:1	Reserved, set to '0x3'		No
	0	Reserved, set to '0'		No

## 9.204 PCH Descriptor Record 203 (Flash Descriptor Records)

Flash Address: FPSBA + 0EDh

Default Flash Address: 1EDh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1EDh	7:0	Reserved, set to '0'		No



## 9.205 PCH Descriptor Record 204 (Flash Descriptor Records)

Flash Address: FPSBA + 0EEh

Default Flash Address: 1EEh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1EEh	7:0	Reserved, set to '0'		No

## 9.206 PCH Descriptor Record 205 (Flash Descriptor Records)

Flash Address: FPSBA + 0EFh

Default Flash Address: 1EFh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1EFh	7:0	Reserved, set to '0'		No

## 9.207 PCH Descriptor Record 206 (Flash Descriptor Records)

Flash Address: FPSBA + 0F0h

Default Flash Address: 1F0h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1F0h	7:2	Reserved, set to '0'		No
	1	<b>BIOS Guard protection override enable (LPC/spi_strap_prr_ts_ovr):</b>  0 = BIOS Guard Fault Tolerant Update Capability is disabled 1 = BIOS guard Fault Tolerant Update Capability is enabled	This setting allows BIOS Guard to bypass the SPI Flash controller protections such as protected range registers and top swap.  <b>Note:</b> For further details please review Intel® Platform Protection Technology with BIOS Guard 2.0 BIOS Specification regarding Fault Tolerant Update (FTU).	Yes
	0	<b>TPM Over SPI Bus Enabled (TOS):</b>  0 = TPM is not on SPI 1 = TPM is on SPI	This field identifies the frequency that should be used with the TPM on SPI. This field is undefined if the TPM on SPI is disabled by softstrap	Yes

## 9.208 PCH Descriptor Record 207 (Flash Descriptor Records)

Flash Address: FPSBA + 0F1h

Default Flash Address: 1F1h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1F1h	7:0	Reserved, set to '0'		No



## 9.209 PCH Descriptor Record 208 (Flash Descriptor Records)

Flash Address: FPSBA + 0F2h

Default Flash Address: 1F2h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1F2h	7:0	Reserved, set to '0'		No

## 9.210 PCH Descriptor Record 209 (Flash Descriptor Records)

Flash Address: FPSBA + 0F3h

Default Flash Address: 1F3h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1F3h	7:0	Reserved, set to '0'		No

## 9.211 PCH Descriptor Record 210 (Flash Descriptor Records)

Flash Address: FPSBA + 0F4h

Default Flash Address: 1F4h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1F4h	7	Reserved, set to '0x1'		No
	6	<b>Intel® PHY Over PCI Express Enable (PHY_PCIE_EN):</b>  0 = Intel integrated wired MAC/PHY communication is not enabled over PCI Express*. 1 = The PCI Express* port selected by the <b>PHY_PCIEPORT_SEL</b> soft strap to be used by Intel® PHY  <b>Note:</b> This bit must be "1" if using Intel integrated wired LAN solution.	This bit MUST be set to '1' if using Intel® integrated wired LAN solution. If not using, or if disabling Intel® integrated wired LAN solution then set this to '0'.	Yes
	5:3	<b>GBE PCIe* Port Select (GBE_PCIEPORTSEL):</b> This strap defines the GbE port.  000 = PORT7 001 = PORT8 010 = PORT9 011 = PORT13 100 = PORT14 101-111 = Reserved	This field tells the PCH which PCI Express* port an Intel® PHY is connected. If PHY_PCIE_EN is = '0', then this field is ignored.  <b>Note:</b> This setting is not the same for all designs, is dependent on the board design. The platform hardware designer or schematic review can determine what PCIe Port the Intel wired PHY is routed.	Yes
	2	<b>DMI / PCIe Port Staggering Enable:</b>  0 = Disabled 1 = Enabled		Yes
	1:0	Reserved, set to '0x1'		No



## 9.212 PCH Descriptor Record 211 (Flash Descriptor Records)

Flash Address: FPSBA + 0F5h

Default Flash Address: 1F5h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1F5h	7:6	Reserved, set to '0'		No
	5:4	<b>SATA /PCIe Combo Port 2 Strap (PCIE_SATA_P2_Flex):</b>  00 = PCIe Port 15 is Statically assigned to SATA Port 1b 01 = PCIe Port 15 is Statically assigned to PCIe (or GbE) 10 = Reserved 11 = Assigned based on the polarity of SATAxPCIE0 determined by PSCPSP_P2_STRP.	This setting determine if PCIe/SATA Comb Port 2 is configured natively for SATA or PCIe.  If the strap setting is configured to '11' the Combo Port behavior is determined by the Combo Port 2Select Polarity strap (PSCPSP_P2_STRP).  <b>Note:</b> The settings for this strap SATA / PCIe Select for Port 1 (SATA_PCIE_SP1) and (SATA_PCIE_GP1) must match for proper port function.  <b>Note:</b> For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe*. These unused SATA/PCIe* Combo Lanes must not be assigned as polarity based.	Yes
	3:2	<b>SATA /PCIe Combo Port 1 Strap (PCIE_SATA_P1_Flex):</b>  00 = PCIe Port 12 is Statically assigned to SATA Port 1a 01 = PCIe Port 12 is Statically assigned to PCIe (or GbE) 10 = Reserved 11 = Assigned based on the polarity for SATAxPCIE1 determined by PSCPSP_P1_STRP	This setting determine if PCIe/SATA Comb Port 1 is configured natively for SATA or PCIe.  If the strap setting is configured to '11' the Combo Port behavior is determined by the Combo Port 1 Select Polarity strap (PSCPSP_P1_STRP).  <b>Note:</b> The settings for this strap and the SATA / PCIe Select for Port 1 (SATA_PCIE_SP1) and (SATA_PCIE_GP1) must match for proper port function.  <b>Note:</b> For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe*. These unused SATA/PCIe* Combo Lanes must not be assigned as polarity based.	Yes



Offset from 0	Bits	Description	Usage	FIT Visible
0x1F5h (Cont)	1:0	<b>SATA /PCIe Combo Port 0 Strap (PCIE_SATA_PO_Flex):</b>  00 = PCIe Port 11 is Statically assigned to SATA Port 0 01 = PCIe Port 11 is Statically assigned to PCIe (or GbE) 10 = Reserved 11 = Assigned based on the polarity for SATAXPCIE0 determined by PSCPSP_PO_STRP.	This setting determine if PCIe/SATA Comb Port 0 is configured natively for SATA or PCIe.  If the strap setting is configured to '11' the Combo Port behavior is determined by the Combo Port 0 Select Polarity strap (PSCPSP_PO_STRP).  <b>Note:</b> The settings for this strap and the SATA / PCIe Select for Port 0 (SATA_PCIE_SPO) and (SATA_PCIE_GPO) must match for proper port function.  <b>Note:</b> For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe*. These unused SATA/PCIe* Combo Lanes must not be assigned as polarity based.	Yes

## 9.213 PCH Descriptor Record 212 (Flash Descriptor Records)

Flash Address: FPSBA + 0F6h

Default Flash Address: 1F6h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1F6h	7:0	Reserved, set to '0'		No

## 9.214 PCH Descriptor Record 213 (Flash Descriptor Records)

Flash Address: FPSBA + 0F7h

Default Flash Address: 1F7h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1F7h	7:0	Reserved, set to '0'		No



## 9.215 PCH Descriptor Record 214 (Flash Descriptor Records)

Flash Address: FPSBA + 0F8h

Default Flash Address: 1F8h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1F8h	7:2	Reserved, set to '0'		No
	1:0	<b>SATA /PCIe Combo Port 3 Strap (PCIE_SATA_P3_Flex):</b>  00 = PCIe Port 16 is Statically assigned to SATA Port 2 01 = PCIe Port 16 is Statically assigned to PCIe (or GbE) 10 = Reserved 11 = Assigned based on the polarity of SATA_PCIE1 determined by PSCPSP_P3_STRP	This setting determine if PCIe/SATA Comb Port 3 is configured natively for SATA or PCIe.  If the strap setting is configured to '11' the Combo Port behavior is determined by the Combo Port 3 Select Polarity strap (PSCPSP_P3_STRP).  <b>Note:</b> The settings for this strap and the SATA / PCIe Select for Port 1 (SATA_PCIE_SP2) and (SATA_PCIE_GP2) must match for proper port function  <b>Note:</b> For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe*. These unused SATA/PCIe* Combo Lanes must not be assigned as polarity based.	Yes

## 9.216 PCH Descriptor Record 215 (Flash Descriptor Records)

Flash Address: FPSBA + 0F9h

Default Flash Address: 1F9h

Offset from 0	Bits	Description	Usage	FIT Visible
0x1F9h	7:0	Reserved, set to '0'		No





## 9.217 PCH Descriptor Record 216 (Flash Descriptor Records)

Flash Address: FPSBA + 0FAh

Default Flash Address: 1FAh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1FAh	7:6	<b>USB3 / PCIe Combo Port 3 (PCIE_USB3_P3_Flex):</b> 00 = Statically assigned to USB3 Port 4 01 = Statically assigned to PCIe Port 4 (or GbE) 10 = Reserved 11 = Reserved	This setting determine if USB3 / PCIe Combo Port 3 is configured natively for USB3 or PCIe.	Yes
	5:4	<b>USB3 / PCIe Combo Port 2 (PCIE_USB3_P2_Flex):</b> 00 = Statically assigned to USB3 Port 3 01 = Statically assigned to PCIe Port 3 (or GbE) 10 = Reserved 11 = Reserved	This setting determine if USB3 / PCIe Combo Port 2 is configured natively for USB3 or PCIe.	Yes
	3:2	<b>USB3 / PCIe Combo Port 1 (PCIE_USB3_P1_Flex):</b> 00 = Statically assigned to USB3 Port 2 01 = Statically assigned to PCIe Port 2 (or GbE) 10 = Reserved 11 = Reserved	This setting determine if USB3 / PCIe Combo Port 1 is configured natively for USB3 or PCIe.	Yes
	1:0	<b>USB3 / PCIe Combo Port 0 (PCIE_USB3_P0_Flex):</b> 00 = Statically assigned to USB3 Port 1 01 = Statically assigned to PCIe Port1 (or GbE) 10 = Reserved 11 = Reserved	This setting determine if USB3 / PCIe Combo Port 0 is configured natively for USB3 or PCIe.	Yes

## 9.218 PCH Descriptor Record 217 (Flash Descriptor Records)

Flash Address: FPSBA + 0FBh

Default Flash Address: 1FBh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1FBh	7:0	Reserved, set to '0'		No



## 9.219 PCH Descriptor Record 218 (Flash Descriptor Records)

Flash Address: FPSBA + 0FCh

Default Flash Address: 1FCh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1FCh	7:4	Reserved, set to '0'		No
	3	<b>Polarity Select SATA / PCIe Combo Port 3 (PSCPSP_P3_STRP):</b>  0x0 = Combo Port 3 is set to PCIe mode when the Combo Port Select pin is '0' and SATA when Combo Port Select pin is '1' 0x1 = Combo Port 3 is set to SATA mode when the Combo Port Select pin is '0' and PCIe when Combo Port Select pin is '1'  <b>Note:</b> This strap is expected to be set to '0x1' when the combo port is mapped to NGFF M.2 or eSATA connector and set to '0x0' when the combo port is mapped to mSATA connector.	This strap is used to determine the configuration the native mode configuration for PCIe/SATA Combo Port 3.  <b>Note:</b> This setting only has effect when PCIe / SATA Combo Port 3 ( <b>PCIE_SATA_P3_Flex</b> ) is configured to '11'  When configuring this strap you must also configure PCIe_SATA GPIO Polarity Port 1 ( <b>SPS1</b> ) to the same setting.	Yes
	2	<b>Polarity Select SATA / PCIe Combo Port 2 (PSCPSP_P2_STRP):</b>  0x0 = Combo Port 2 is set to PCIe mode when the Combo Port Select pin is '0' and SATA when Combo Port Select pin is '1' 0x1 = Combo Port 2 is set to SATA mode when the Combo Port Select pin is '0' and PCIe when Combo Port Select pin is '1'  <b>Note:</b> This strap is expected to be set to '0x1' when the combo port is mapped to NGFF M.2 or eSATA connector and set to '0x0' when the combo port is mapped to mSATA connector.	This strap is used to determine the configuration the native mode configuration for PCIe/SATA Combo Port 3.  <b>Note:</b> This setting only has effect when PCIe / SATA Combo Port 2 ( <b>PCIE_SATA_P3_Flex</b> ) is configured to '11'  When configuring this strap you must also configure SATA /PCIe GPIO Polarity Port 0 ( <b>SPS0</b> ) to the same setting.	Yes
	1	<b>Polarity Select SATA / PCIe Combo Port 1 (PSCPSP_P1_STRP):</b>  0x0 = Combo Port 1 is set to PCIe mode when the Combo Port Select pin is '0' and SATA when Combo Port Select pin is '1' 0x1 = Combo Port 1 is set to SATA mode when the Combo Port Select pin is '0' and PCIe when Combo Port Select pin is '1'  <b>Note:</b> This strap is expected to be set to '0x1' when the combo port is mapped to NGFF M.2 or eSATA connector and set to '0x0' when the combo port is mapped to mSATA connector.	This strap is used to determine the configuration the native mode configuration for PCIe/SATA Combo Port 1.  <b>Note:</b> This setting only has effect when PCIe / SATA Combo Port 1 ( <b>PCIE_SATA_P1_Flex</b> ) is configured to '11'  When configuring this strap you must also configure SATA /PCIe GPIO Polarity Port 1 ( <b>SPS1</b> ) to the same setting.	Yes



Offset from 0	Bits	Description	Usage	FIT Visible
0x1FCh (cont)	0	<b>Polarity Select SATA / PCIe Combo Port 0 (PSCPSP_PO_STRP):</b>  0x0 = Combo Port 0 is set to PCIe mode when the Combo Port Select pin is '0' and SATA when Combo Port Select pin is '1' 0x1 = Combo Port 0 is set to SATA mode when the Combo Port Select pin is '0' and PCIe when Combo Port Select pin is '1'  <b>Note:</b> This strap is expected to be set to '0x1' when the combo port is mapped to NGFF M.2 or eSATA connector and set to '0x0' when the combo port is mapped to mSATA connector.	This strap is used to determine the configuration the native mode configuration for PCIe/SATA Combo Port 0.  <b>Note:</b> This setting only has effect when SATA / PCIe Combo Port 0 ( <b>SATA_PCIE_PO_Flex</b> ) is configured to '11'  When configuring this strap you must also configure SATA /PCIe GPIO Polarity Port 0 ( <b>SPS0</b> ) to the same setting.	Yes

## 9.220 PCH Descriptor Record 219 (Flash Descriptor Records)

Flash Address: FPSBA + 0FDh

Default Flash Address: 1FDh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1FDh	7:0	Reserved, set to '0'		No

## 9.221 PCH Descriptor Record 220 (Flash Descriptor Records)

Flash Address: FPSBA + 0FEh

Default Flash Address: 1FEh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1FEh	7:0	Reserved, set to '0'		No



## 9.222 PCH Descriptor Record 221 (Flash Descriptor Records)

Flash Address: FPSBA + 0FFh

Default Flash Address: 1FFh

Offset from 0	Bits	Description	Usage	FIT Visible
0x1FFh	7:6	<b>USB3 / PCIe Combo Port 5 (PCI_E_USB3_P3_Flex):</b> 00 = Statically assigned to USB3 Port 6 01 = Statically assigned to PCIe Port 6 (or GbE) 10 = Reserved 11 = Reserved	This setting determine if USB3 / PCIe Combo Port 5 is configured natively for USB3 or PCIe.	Yes
	5:4	<b>USB3 / PCIe Combo Port 4 (PCI_E_USB3_P2_Flex):</b> 00 = Statically assigned to USB3 Port 5 01 = Statically assigned to PCIe Port 5 (or GbE) 10 = Reserved 11 = Reserved	This setting determine if USB3 / PCIe Combo Port 4 is configured natively for USB3 or PCIe.	Yes
	3:0	Reserved, set to '0'		No

## 9.223 PCH Descriptor Record 222 (Flash Descriptor Records)

Flash Address: FPSBA + 100h

Default Flash Address: 200h

Offset from 0	Bits	Description	Usage	FIT Visible
0x200h	7:0	Reserved, set to '0'		No

## 9.224 PCH Descriptor Record 223 (Flash Descriptor Records)

Flash Address: FPSBA + 101h

Default Flash Address: 201h

Offset from 0	Bits	Description	Usage	FIT Visible
0x201h	7:0	Reserved, set to '0'		No



## 9.225 PCH Descriptor Record 224 (Flash Descriptor Records)

Flash Address: FPSBA + 102h

Default Flash Address: 202h

Offset from 0	Bits	Description	Usage	FIT Visible
0x202h	7:0	Reserved, set to '0x1'		No

## 9.226 PCH Descriptor Record 225 (Flash Descriptor Records)

Flash Address: FPSBA + 103h

Default Flash Address: 203h

Offset from 0	Bits	Description	Usage	FIT Visible
0x203h	7:3	Reserved, set to '0'		No
	2	<b>SATA / PCIe Combo Port 2 Mode Select (CLKREQ2_DEVS_LP2_MODE):</b>  0 = SATA / PCIe Combo Port 2 mode configured as PCIe CLKREQ# 1 = SATA / PCIe Combo Port 2 mode configured as SATA DEVS_LP#	The corresponding CLKREQ# GPIO can only function as DEVS_LP# if PCIe/SATA Combo Port 2 is assigned to SATA, and SATA / PCIe Combo Port 2 Mode Select is configured to SATA DEVS_LP#.	Yes
	1	<b>SATA / PCIe Combo Port 1 Mode Select (CLKREQ1_DEVS_LP1_MODE):</b>  0 = SATA / PCIe Combo Port 1 mode configured as PCIe CLKREQ# 1 = SATA / PCIe Combo Port 1 mode configured as SATA DEVS_LP#	The corresponding CLKREQ# GPIO can only function as DEVS_LP# if PCIe/SATA Combo Port 1 is assigned to SATA, and SATA / PCIe Combo Port 1 Mode Select is configured to SATA DEVS_LP#.	Yes
	0	<b>SATA / PCIe Combo Port 0 Mode Select (CLKREQ0_DEVS_LP0_MODE):</b>  0 = SATA / PCIe Combo Port 0 mode configured as PCIe CLKREQ# 1 = SATA / PCIe Combo Port 0 mode configured as SATA DEVS_LP#	The corresponding CLKREQ# GPIO can only function as DEVS_LP# if PCIe/SATA Combo Port 0 is assigned to SATA, and SATA / PCIe Combo Port 0 Mode Select is configured to SATA DEVS_LP#.	Yes



## 9.227 PCH Descriptor Record 226 (Flash Descriptor Records)

Flash Address: FPSBA + 104h

Default Flash Address: 204h

Offset from 0	Bits	Description	Usage	FIT Visible
0x204h	7:6	Reserved, set to '0'		No
	5:4	<b>SATA / PCIe Select for Port 2 (SATA_PCIE_SP2):</b>  00 = PCIe Port 16 is statically assigned to SATA Port 2 01 = PCIe Port 16 is statically assigned to PCIe (or GbE) 10 = Reserved 11 = Assigned based on the polarity of SATAxPCIEx2 determined by SPS2	This strap must also be configured when setting the PCIe / SATA Combo Port 4 (PCIE_SATA_P3_Flex).  <b>Note:</b> This strap and the PCIe / SATA Combo Port 4 (PCIE_SATA_P3_Flex) and (SATA_PCIE_GP2) must match for proper port function.  <b>Note:</b> For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe*. These unused SATA/PCIe* Combo Lanes must not be assigned as polarity based.	No
	3:2	<b>SATA / PCIe Select for Port 1 (SATA_PCIE_SP1):</b>  00 = PCIe Port 12 or PCIe Port 15 is statically assigned to SATA Port 1 01 = PCIe Port 12 or PCIe Port 15 is statically assigned to PCIe (or GbE) 10 = Reserved 11 = Assigned based on the polarity of SATAxPCIEx1 determined by SPS1	This strap must also be configured when setting the PCIe / SATA Combo Port 1 Strap (PCIE_SATA_P1_Flex) or SATA / PCIe Combo Port 3 Strap (PCIE_SATA_P2_Flex).  <b>Note:</b> This strap and the PCIe / SATA Combo Port 1 Strap (PCIE_SATA_P1_Flex) or PCIe / SATA Combo Port 3 Strap (PCIE_SATA_P2_Flex) and (SATA_PCIE_GP1) must match for proper port function.  <b>Note:</b> For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe*. These unused SATA/PCIe* Combo Lanes must not be assigned as polarity based.	No
	1:0	<b>SATA / PCIe Select for Port 0 (SATA_PCIE_SP0):</b>  00 = PCIe Port 11 is statically assigned to SATA Port 0 01 = PCIe Port 11 is statically assigned to PCIe (or GbE) 10 = Reserved 11 = Assigned based on the polarity of SATAxPCIEx0 determined by SPS0	This strap must also be configured when setting the PCIe / SATA Combo Port 0 (PCIE_SATA_P0_Flex).  <b>Note:</b> This strap and the PCIe / SATA Combo Port 0 (PCIE_SATA_P0_Flex) and (SATA_PCIE_GP0) must match for proper port function.  <b>Note:</b> For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe*. These unused SATA/PCIe* Combo Lanes must not be assigned as polarity based.	No



## 9.228 PCH Descriptor Record 227 (Flash Descriptor Records)

Flash Address: FPSBA + 105h

Default Flash Address: 205h

Offset from 0	Bits	Description	Usage	FIT Visible
0x205h	7:0	Reserved, set to '0x55'		No

## 9.229 PCH Descriptor Record 228 (Flash Descriptor Records)

Flash Address: FPSBA + 106h

Default Flash Address: 206h

Offset from 0	Bits	Description	Usage	FIT Visible
0x206h	7:3	Reserved, set to '0'		No
	2	<b>SATA / PCIe GPIO Polarity Port 2 (SPS2)</b>  0x0 = GPIO Polarity Port 2 is set to PCIe mode when the SATAXPCE2 pin is '0' and SATA when SATAXPCE2 pin is '1' 0x1 = GPIO Polarity Port 2 is set to SATA mode when the SATAXPCE2 pin is '0' and PCIe when SATAXPCE2 pin is '1'	This strap must also be configured if PCIe/ <b>SATA Combo Port 3 Strap</b> (PCIE_SATA_P3_Flex) is configured to '11'  Note: This setting only has effect when SATA / PCIe Select for Port 2 (SATA_PCIE_SP2) is configured to '11'  Note: This strap and the Polarity Select SATA / PCIe Combo Port 4 (PSCPSP_P3_STRP) must match for proper port function.	No
	1	<b>SATA / PCIe GPIO Polarity Port 1 (SPS1)</b>  0x0 = GPIO Polarity Port 1 is set to PCIe mode when the SATAXPCE1 pin is '0' and SATA when SATAXPCE1 pin is '1' 0x1 = GPIO Polarity Port 1 is set to SATA mode when the SATAXPCE1 pin is '0' and PCIe when SATAXPCE1 pin is '1'	This strap must also be configured if PCIe/ <b>SATA Combo Port 1 strap</b> (PCIE_SATA_P1_Flex) or <b>SATA Combo Port 2</b> (PCIE_SATA_P2_Flex) is configured to '11'  Note: This setting only has effect when SATA / PCIe Select for Port 1 (SATA_PCIE_SP1) is configured to '11'  Note: This strap and the Polarity Select SATA / PCIe Combo Port 1 (PSCPSP_P1_STRP) or Polarity Select SATA / PCIe Combo Port 2 (PSCPSP_P2_STRP) must match for proper port function.	No
	0	<b>SATA / PCIe GPIO Polarity Port 0 (SPS0)</b>  0x0 = GPIO Polarity Port 0 is set to PCIe mode when the SATAXPCE0 pin is '0' and SATA when SATAXPCE0 pin is '1' 0x1 = GPIO Polarity Port 0 is set to SATA mode when the SATAXPCE0 pin is '0' and PCIe when SATAXPCE0 pin is '1'	This strap must also be configured if PCIe/ <b>SATA Combo Port 0 strap</b> (PCIE_SATA_PO_Flex) is configured to '11'  Note: This setting only has effect when SATA / PCIe Select for Port 0 (SATA_PCIE_SPO) is configured to '11'  Note: This strap and the Polarity Select SATA / PCIe Combo Port 0 (PSCPSP_PO_STRP) must match for proper port function.	No



## 9.230 PCH Descriptor Record 229 (Flash Descriptor Records)

Flash Address: FPSBA + 107h

Default Flash Address: 207h

Offset from 0	Bits	Description	Usage	FIT Visible
0x207h	7:0	Reserved, Set to '0'		No

## 9.231 PCH Descriptor Record 230 (Flash Descriptor Records)

Flash Address: FPSBA + 108h

Default Flash Address: 208h

Offset from 0	Bits	Description	Usage	FIT Visible
0x208h	7:2	Reserved, Set to '0x24'		No
	1:0	Reserved, Set to '0x3'		No

## 9.232 PCH Descriptor Record 231 (Flash Descriptor Records)

Flash Address: FPSBA + 109h

Default Flash Address: 209h

Offset from 0	Bits	Description	Usage	FIT Visible
0x209h	7	Reserved, Set to '0x1'		No
	6:0	Reserved, Set to '0x70'		No

## 9.233 PCH Descriptor Record 232 (Flash Descriptor Records)

Flash Address: FPSBA + 10Ah

Default Flash Address: 20Ah

Offset from 0	Bits	Description	Usage	FIT Visible
0x20Ah	7:3	Reserved, set to '0x1'		No
	2:0	<b>PHY Connection (PHYCON):</b> This field determines if Intel® wired PHY is connected.  000 = No PHY connected 001 = PHY on SMBus 010 = PHY on SMLink0 011 = PHY on SMLink1	This field must be set to "10" if Intel integrated wired LAN solution is used. If not using, or if disabling Intel integrated wired LAN solution, then field must be set to "00".	Yes





## 9.234 PCH Descriptor Record 233 (Flash Descriptor Records)

Flash Address: FPSBA + 10Bh

Default Flash Address: 20Bh

Offset from 0	Bits	Description	Usage	FIT Visible
0x20Bh	7:4	Reserved, set to '0xf'		No
	3:2	Reserved, set to '0x3'		No
	1:0	Reserved, set to '0x3'		No

## 9.235 PCH Descriptor Record 234 (Flash Descriptor Records)

Flash Address: FPSBA + 10Ch

Default Flash Address: 20Ch

Offset from 0	Bits	Description	Usage	FIT Visible
0x20Ch	7:4	Reserved, set to '0xf'		No
	3	Reserved, set to '0'		No
	2	Reserved, set to '0x1'		No
	1:0	Reserved, set to '0'		No

## 9.236 PCH Descriptor Record 235 (Flash Descriptor Records)

Flash Address: FPSBA + 10Dh

Default Flash Address: 20Dh

Offset from 0	Bits	Description	Usage	FIT Visible
0x20Dh	7:2	Reserved, set to '0x3f'		No
	1:0	Reserved, set to '0'		No

## 9.237 PCH Descriptor Record 236 (Flash Descriptor Records)

Flash Address: FPSBA + 10Eh

Default Flash Address: 20Eh

Offset from 0	Bits	Description	Usage	FIT Visible
0x20Eh	7:0	Reserved, set to '0xfc'		No



## 9.238 PCH Descriptor Record 237 (Flash Descriptor Records)

Flash Address: FPSBA + 10Fh

Default Flash Address: 20Fh

Offset from 0	Bits	Description	Usage	FIT Visible
0x20Fh	7:2	Reserved, set to '0x3f'		No
	1:0	Reserved, set to '0'		No

## 9.239 PCH Descriptor Record 238 (Flash Descriptor Records)

Flash Address: FPSBA + 110h

Default Flash Address: 210h

Offset from 0	Bits	Description	Usage	FIT Visible
0x210h	7:0	Reserved, set to '0x1'		No

## 9.240 PCH Descriptor Record 239 (Flash Descriptor Records)

Flash Address: FPSBA + 111h

Default Flash Address: 211h

Offset from 0	Bits	Description	Usage	FIT Visible
0x211h	23:0	Reserved, set to '0'		No



## 9.241 MIP Table Descriptor Record 0 (Flash Descriptor Records)

Flash Address: MDTBA + 000h

Default Flash Address: C00h

Offset from 0	Bits	Description	Usage	FIT Visible
0xC00h	15:0	<b>Number of MIP Table Descriptor Entries:</b> Set to '0x2'	This setting determines the total number of MIP Table Descriptor entries present in the SPI image.	No

## 9.242 MIP Table Descriptor Record 1 (Flash Descriptor Records)

Flash Address: MDTBA + 002h

Default Flash Address: C02h

Offset from 0	Bits	Description	Usage	FIT Visible
0xC02h	15:0	<b>Size of MIP Descriptor Entry:</b> Set to '0x44'	This setting determines the size in bytes of the MIP Descriptor Entry structure.	No

## 9.243 MIP Table Descriptor Record 2 (Flash Descriptor Records)

Flash Address: MDTBA + 004h

Default Flash Address: C04h

Offset from 0	Bits	Description	Usage	FIT Visible
0xC04h	15:0	<b>MIP Descriptor Block 0:</b> Set to '0x1'	This setting determines what the data type is for the MIP Descriptor.	No

## 9.244 MIP Table Descriptor Record 3 (Flash Descriptor Records)

Flash Address: MDTBA + 006h

Default Flash Address: C06h

Offset from 0	Bits	Description	Usage	FIT Visible
0xC06h	15:0	<b>MIP Descriptor Block 0 Offset:</b> Set to '0x14'	This setting determines the offset location of the MIP Descriptor Table Entries.	No



## 9.245 MIP Table Descriptor Record 4 (Flash Descriptor Records)

Flash Address: MDTBA + 008h

Default Flash Address: C08h

Offset from 0	Bits	Description	Usage	FIT Visible
0xC08h	15:0	<b>MIP Descriptor Block 0 Length:</b> Set to '0x28'	This setting determine the length of the MIP Descriptor Block 0.	No

## 9.246 MIP Table Descriptor Record 5 (Flash Descriptor Records)

Flash Address: MDTBA + 00Ah

Default Flash Address: C1Ah

Offset from 0	Bits	Description	Usage	FIT Visible
0xC0Ah	15:0	Reserved, set to '0'		No

## 9.247 MIP Table Descriptor Record 6 (Flash Descriptor Records)

Flash Address: MDTBA + 00Ch

Default Flash Address: C0Ch

Offset from 0	Bits	Description	Usage	FIT Visible
0xC0Ch	15:0	<b>MIP Descriptor Block 1 Type:</b> Set to '0'	This setting determines what the data type is for the MIP Descriptor.	No

## 9.248 MIP Table Descriptor Record 7 (Flash Descriptor Records)

Flash Address: MDTBA + 00Eh

Default Flash Address: C0Eh

Offset from 0	Bits	Description	Usage	FIT Visible
0xC0Eh	15:0	<b>MIP Descriptor Block 1 Offset:</b> Set to '0x3C'	This setting determines the offset location of the MIP Descriptor Table Entries.	No



## 9.249 MIP Table Descriptor Record 8 (Flash Descriptor Records)

Flash Address: MDTBA + 010h

Default Flash Address: C10h

Offset from 0	Bits	Description	Usage	FIT Visible
0xC10h	15:0	<b>MIP Descriptor Block 1 Length:</b> Set to '0x8'	This setting determine the length of the MIP Descriptor Block 1.	No

## 9.250 MIP Table Descriptor Record 9 (Flash Descriptor Records)

Flash Address: MDTBA + 012h

Default Flash Address: C12h

Offset from 0	Bits	Description	Usage	FIT Visible
0xC12h	15:0	Reserved, set to '0'		No



## 9.251 PMC Descriptor Record 0 (Flash Descriptor Records)

Flash Address: MDTBA + 014h

Default Flash Address: C14h

Offset from 0	Bits	Description	Usage	FIT Visible
0xC14h	31:28	Reserved, set to '0'		No
	27	<b>Intel® Trace Hub Debug Messages Enable:</b>  0 = PCH Tracing debug messages Disabled 1 = PCH Tracing debug messages Enabled	This setting enables debug messages on the Intel® Trace Hub.  <b>Note:</b> You will also need to set the Intel® Trace Hub Soft Enable to "Enabled"	Yes
	26	Reserved, set to '0'		No
	25	<b>Thermal Power Reporting Enable (THERM_PWR_REP_DIS):</b>  0 = Thermal Power Reporting is enabled. 1 = Thermal Power Reporting is completely disabled, regardless of the settings in the Thermal Power Reporting configuration registers.  <b>Note:</b> When this setting is disabled the once-per-second timer interrupt associated with this feature must not be turned on.	This bit, when set, causes the PMC FW to completely turn off the Thermal Power Reporting feature.  <b>Note:</b> A once-per-second timer interrupt is enabled which triggers firmware to report power and temperature information as enabled by configuration registers.	Yes
	24	<b>PCIe* Power Stable Timer (tPCH33 timer):</b>  0 = tPCH33 timer is disabled 1 = PCH will count 99ms from PWROK assertion before PLTRST# is de-asserted.	Board dependent. Default is disabled, Platform is required to ensure timing of PWROK and SYS_PWROK in such a way that it satisfies the PCIe timing requirement of power stable to reset de-assertion.	Yes
	23	Reserved, set to '0'		No
	21:20	<b>APWROK Timing (APWROK_TIMING):</b>  00 = 2 ms 01 = 4 ms 10 = 8 ms 11 = 16 ms	This soft strap determines the time between the SLP_A# pin de-asserting and the APWROK timer expiration.	Yes
	20	<b>DeepSx Platform Configuration (DEEPSX_PLT_CFG_SS):</b>  0 = The platform does not support DeepSx. 1 = The platform supports DeepSx	This setting and <b>Deep Sx Enable (Deep_SX_EN)</b> must match for proper operation of the Deep Sx feature.	No
	19	<b>LAN PHY Power Up Time (LAN_PHY_PU_TIME):</b>  0 = 100ms 1 = 50ms	This bit determines how long the delay for LAN PHY to power up after de-assertion of SLP_LAN#.	Yes
	18:15	Reserved, set to '0'		No
	14	<b>Type-C Default State (TYPE_C_STATE):</b>  0 = USB SPR in un-subscription or disconnected state by default. 1 = USB SPR in host subscription state by default.	This setting configures the default state for Type-C connectors.  <b>Note:</b> When configured to USB SPR in host subscription state all Type-C port connection / disconnection is handled through PMC.	No
	13:12	Reserved, set to '0'		No



Offset from 0	Bits	Description	Usage	FIT Visible
0xC14h (cont)	11:10	<b>tPCH46 Timing:</b>  00 = 1 ms 01 = Reserved 10 = 5 ms 11 = 2 ms	tPch46: PROCPWRGD and SYS_PWROK high to SUS_STAT# deassertion. Refer to EDS for details.	Yes
	9:8	<b>tPCH45 Timing:</b>  00 = 100 ms 01 = 50 ms 10 = 5 ms 11 = 1 ms	tPCH45: PCH clock output stable to PROCPWRGD high. Refer to EDS for details.	Yes
	7:0	Reserved, set to '0x3e'		No

## 9.252 PMC Descriptor Record 1 (Flash Descriptor Records)

Flash Address:MDTBA + 018h

Default Flash Address: C18h

Offset from 0	Bits	Description	Usage	FIT Visible
0xC18h	31:8	Reserved, set to '0'		No
	7	<b>Integrated Sensor Hub Supported:</b>  0 = Enable Integrated Sensor Hub 1 = Disable Integrated Sensor Hub		Yes
	6:1	Reserved, set to '0'		No
	0	<b>Intel® Integrated wired LAN Enable (IWL_EN):</b>  0 = Enabled Intel® Integrated wired LAN Solution 1 = Disabled Intel® Integrated wired LAN Solution  <b>Note:</b> This must be set to '0' if the platform is using Intel's integrated wired LAN solution. Set to '1' if not using Intel integrated wired LAN solution or if disabling it.	This must be set to '0' if the platform is using the Intel® Integrated wired LAN solution. This must be set to '1' if not using the Intel® Integrated wired LAN solution or if disabling it.	Yes

## 9.253 PMC Descriptor Record 2 (Flash Descriptor Records)

Flash Address:MDTBA + 01Ch

Default Flash Address: C1Ch

Offset from 0	Bits	Description	Usage	FIT Visible
0xC1Ch	31:0	Reserved, set to '0x43C9B810'		No



## 9.254 PMC Descriptor Record 3 (Flash Descriptor Records)

Flash Address: MDTBA + 020h

Default Flash Address: C20h

Offset from 0	Bits	Description	Usage	FIT Visible
0xC20h	31:0	Reserved, set to '0x5C40'		No

## 9.255 PMC Descriptor Record 4 (Flash Descriptor Records)

Flash Address: MDTBA + 024h

Default Flash Address: C24h

Offset from 0	Bits	Description	Usage	FIT Visible
0xC24h	31:18	Reserved, set to '0'		No
	17	SLP_S0# Tunnel (SLP_S0_TUNNEL_DIS):  0 = SLP_S0# Tunnel enabled 1 = SLP_S0# Tunnel disabled	This setting enables / disabled the SLP_S0# tunneling over the eSPI to EC interface.  <b>Note:</b> On eSPI enabled platforms this should be set to disabled for proper Sleep S0 operation.	Yes
	16:11	Reserved, set to '0'		No
	10:9	OPI Link Voltage Strap (OPD_LVO_STRP):  0x0 = 0.85 Volts 0x1 = 0.95 Volts 0x2 = 1.05 Volts	This strap must be configured when setting OPI Link Voltage strap (OPD_LVO).  <b>Note:</b> This strap and the OPI Link Voltage strap (OPD_LVO) must match the same voltage configuration setting for proper platform operation function.	No
	8	OPI Link Speed Strap (OPDMI_STRP):  0x0 = 2 / GT/s Link Speed 0x1 = 4 / GT/s Link Speed	This strap must be configured when setting OPI Link Speed strap (OPDMI_TLS).  <b>Note:</b> This strap and the OPI Link Speed strap (OPDMI_TLS) must match the same GT configuration setting for proper platform operation function.	No
	7:2	Reserved, set to '0'		No
0xC24h (Cont)	1	CLKOUT_CPUSSC_P/N Clock Path Generation:  0 = HDA_PLL Path 1 = Direct XTAL_IN/OUT Path	This setting determines if CLKOUT_CPUSSC_P/N Clock Path is generated through the HDA_PLL or from Direct XTAL IN/OUT.	Yes
	0	Reserved, set to '0'		No





## 9.256 PMC Descriptor Record 5 (Flash Descriptor Records)

Flash Address: MDTBA + 028h

Default Flash Address: C28h

Offset from 0	Bits	Description	Usage	FIT Visible
0xC28h	31:15	Reserved, set to '0'		No
	14:8	Reserved, set to '0x64'		No
	7:0	Reserved, set to '0'		No



## 9.257 CPU Descriptor Record 0 (Flash Descriptor Records)

Flash Address: MDTBA + 02Ch

Default Flash Address: C2Ch

Offset from 0	Bits	Description	Usage	FIT Visible
0xC2Ch	31:27	<b>CPU Strap Length (CPUSL):</b>  Identifies the 1's based number of Dwords of Processor Straps to be read, up to 31 DWs (1KB) max. A setting of all 0's indicates there are no Processor DW straps.  <b>Set this field to 0x3h</b>		No
	26:0	Reserved, set to '0'		No



## 9.258 CPU Descriptor Record 1 (Flash Descriptor Records)

Flash Address: MDTBA + 030h

Default Flash Address: C30h

Offset from 0	Bits	Description	Usage	FIT Visible
0xC30h	31:14	Reserved, set to '0x0'		No
	13	<b>JTAG Power Disable:</b> 0 = Disable JTAG Power for C10 and deeper states 1 = Enable JTAG Power for C10 and deeper states	This setting determines if JTAG power will be maintained on C10 or lower power states.  <b>Note:</b> This strap is intended for debugging purposed only.	Yes
	12	<b>Processor Boot Max Frequency:</b> 0 = Disable Boot Max Frequency 1 = Enable Boot Max Frequency	This setting determines if the processor will operate at maximum frequency at power-on and boot.  <b>Note:</b> This strap is intended for debugging purposed only.	Yes
	11:6	<b>Flex Ratio:</b> '0x0'	This setting controls the maximum processor non-turbo ratio.  <b>Note:</b> This strap is intended for debugging purposed only. See BIOS Spec for more details on maximum processor non-turbo ratio configuration.	Yes
	5	<b>BIST Initialization:</b> 0 = Disable BIST at Reset 1 = Enable BIST at Reset	This setting determines if BIST will be run at platform reset after BIOS requested actions.  <b>Note:</b> This strap is intended for debugging purposed only.	Yes
	4	Reserved, set to '0x0'		No
	3:1	<b>Number of Active Cores:</b> 0 = All Cores active 1 = One core active 2 = Two cores active 3 = Three cores active 4 = Four cores active	This setting controls the number of active processor cores.  <b>Note:</b> This strap is intended for debugging purposed only. See BIOS Spec for more details on enabling / disabling processor cores.	Yes
	0	<b>Disable Hyper threading:</b> 0 = Enable Hyper Threading 1 = Disable Hyper Threading	This setting control enabling / disabling of Hyper threading.  <b>Note:</b> This strap is intended for debugging purposed only. See BIOS Spec for more details on enabling / disabling Hyper threading	Yes



## 9.259 CPU Descriptor Record 2 (Flash Descriptor Records)

Flash Address: MDTBA + 034h

Default Flash Address: C34h

Offset from 0	Bits	Description	Usage	FIT Visible
0xC34h	31	<b>Platform IMON:</b> 0 = IMON enabled 1 = IMON disabled	<b>Note:</b> This strap should be left at the recommended default setting.	Yes
	30	<b>SVID Presence:</b> 0 = SVID is present 1 = No SVID is present	This setting determine if SVID rails are present on the platform. See Processor EDS for details.	Yes
	29:25	<b>Reserved, set to '0'</b>		No
	24	<b>GT_S VR Type:</b> 0 = GT slice domain VR type SVID 1 = GT slice domain VR type is fixed VR	This setting determines the GT slice domain VR type. See Processor EDS for details.	Yes
	23:20	<b>GT_S Power Plane Topology:</b> '0x1'	This setting determines the GT slice power plane topology. See Processor EDS for details.  <b>Note:</b> This strap should be left at the recommended default setting.	Yes
	19	<b>GT_US VR Type:</b> 0 = GT Unslice domain VR type SVID 1 = GT Unslice domain VR type is fixed VR	This setting determines the GT Unslice domain VR type. See Processor EDS for details.	Yes
	18:15	<b>GT_US Power Plane Topology:</b> '0x1'	This setting determines the GT Unslice power plane topology. See Processor EDS for details.  <b>Note:</b> This strap should be left at the recommended default setting.	Yes
	14	<b>Ring VR Type:</b> 0 = Ring domain VR Type SVID 1 = Ring domain VR type is fixed VR	This setting determines the Ring domain VR type. See Processor EDS for details.	Yes
	13:10	<b>Ring Power Plane Topology:</b> '0x0'	This setting determines the Ring power plane topology. See Processor EDS for details.  <b>Note:</b> This strap should be left at the recommended default setting.	Yes
	9	<b>IA Power Plane VR:</b> 0 = IA core domain VR Type SVID 1 = IA core domain VR type is fixed VR	This setting determines the IA core domain VR type. See Processor EDS for details.	Yes
	8:5	<b>IA Power Plane Topology:</b> '0x0'	This setting determines the IA power plane topology. See Processor EDS for details.  <b>Note:</b> This strap should be left at the recommended default setting.	Yes



Offset from 0	Bits	Description	Usage	FIT Visible
0xC34h (cont)	4	<b>SA VR Type:</b>  0 = SA core domain VR Type SVID 1 = SA core domain VR type is fixed VR	This setting determines the SA core domain VR type. See Processor EDS for details.	Yes
	3:0	<b>SA Power Plane Topology:</b>  '0x2'	This setting determines the SA power plane topology. See Processor EDS for details.  <b>Note:</b> This strap should be left at the recommended default setting.	Yes



## 9.260 CPU Descriptor Record 3 (Flash Descriptor Records)

Flash Address: MDTBA + 038h

Default Flash Address: C38h

Offset from 0	Bits	Description	Usage	FIT Visible
0xC38h	31:28	<b>SE Key Mode:</b> '0x0'	<b>Note:</b> This strap should be left at the recommended default setting.	Yes
	27	Reserved set to '0x1'		No
	26:10	Reserved set to '0'		No
	9	<b>EDRAM VR Type:</b> 0 = EDRAM core domain VR Type SVID 1 = EDRAM core domain VR type is fixed VR	This setting determines the eOPPIO domain VR type. See Processor EDS for details.	Yes
	8:5	<b>EDRAM Power Plane Topology:</b> '0x0'	This setting determines the EDRAM power plane topology. See Processor EDS for details.  <b>Note:</b> This strap should be left at the recommended default setting.	Yes
	4	<b>eOPPIO VR Type:</b> 0 = eOPPIO domain VR Type SVID 1 = eOPPIO core domain VR type is fixed VR	This setting determines the eOPPIO domain VR type. See Processor EDS for details.	Yes
	3:0	<b>eOPPIO Power Plane Topology:</b> '0x0005'	This setting determines the eOPPIO power plane topology. See Processor EDS for details.  <b>Note:</b> This strap should be left at the recommended default setting.	Yes



## 9.261 Intel® ME Descriptor Record 0 (Flash Descriptor Records)

Flash Address: MDTBA + 03Ch

Default Flash Address: C3Ch

Offset from 0	Bits	Description	Usage	FIT Visible
0xC3Ch	31:20	Reserved, set to '0'		No
	19:18	<b>USB2 Port 10 DbC AFE Signal Strength:</b>  0x0 – Unused 0x1 – Weak 0x2 – Medium 0x3 – Strong	This setting determines the DbC Analog Front End signal strength for USB2 port 10.	Yes
	17:16	<b>USB2 Port 9 DbC AFE Signal Strength:</b>  0x0 – Unused 0x1 – Weak 0x2 – Medium 0x3 – Strong	This setting determines the DbC Analog Front End signal strength for USB2 port 9.	Yes
	15:14	<b>USB2 Port 8 DbC AFE Signal Strength:</b>  0x0 – Unused 0x1 – Weak 0x2 – Medium 0x3 – Strong	This setting determines the DbC Analog Front End signal strength for USB2 port 8.	Yes
	13:12	<b>USB2 Port 7 DbC AFE Signal Strength:</b>  0x0 – Unused 0x1 – Weak 0x2 – Medium 0x3 – Strong	This setting determines the DbC Analog Front End signal strength for USB2 port 7.	Yes
	11:10	<b>USB2 / USB3 Port 6 DbC AFE Signal Strength:</b>  0x0 – Unused 0x1 – Weak 0x2 – Medium 0x3 – Strong	This setting determines the DbC Analog Front End signal strength for USB2 / USB3 port 6.	Yes
	9:8	<b>USB2 / USB3 Port 5 DbC AFE Signal Strength:</b>  0x0 – Unused 0x1 – Weak 0x2 – Medium 0x3 – Strong	This setting determines the DbC Analog Front End signal strength for USB2 / USB3 port 5.	Yes



Offset from 0	Bits	Description	Usage	FIT Visible
0xC3Ch (Cont)	7:6	<b>USB2 / USB3 Port 4 DbC AFE Signal Strength:</b>  0x0 – Unused 0x1 – Weak 0x2 – Medium 0x3 – Strong	This setting determines the DbC Analog Front End signal strength for USB2 / USB3 port 4.	Yes
	5:4	<b>USB2 / USB3 Port 3 DbC AFE Signal Strength:</b>  0x0 – Unused 0x1 – Weak 0x2 – Medium 0x3 – Strong	This setting determines the DbC Analog Front End signal strength for USB2 / USB3 port 3.	Yes
	3:2	<b>USB2 / USB3 Port 2 DbC AFE Signal Strength:</b>  0x0 – Unused 0x1 – Weak 0x2 – Medium 0x3 – Strong	This setting determines the DbC Analog Front End signal strength for USB2 / USB3 port 2.	Yes
	1:0	<b>USB2 / USB3 Port 1 DbC AFE Signal Strength:</b>  0x0 – Unused 0x1 – Weak 0x2 – Medium 0x3 – Strong	This setting determines the DbC Analog Front End signal strength for USB2 / USB3 port 1.	Yes





## 9.262 Intel® ME Descriptor Record 1 (Flash Descriptor Records)

Flash Address: MDTBA + 040h

Default Flash Address: C40h

Offset from 0	Bits	Description	Usage	FIT Visible
0xC40h	31:25	Reserved, set to '0'		No
	24	<b>Delayed Authentication Mode enable (DAM_EN):</b>  0x0 = DAM is disabled 0x1 = DAM is enabled	This setting Enables / Disables Delayed Authentication Mode on the platform.	No
	23:16	<b>Early USB DbC Intel® ME Boot Stall Enable:</b>  0 = Intel® ME Boot Stall not enabled 1 = Intel® ME Boot Stall enabled	This setting enables a delay during Intel® ME FW bring-up to allow USB DCI to be established and Early DbC arbitration to be granted.	Yes
	15:8	<b>USB3 DbC port enable:</b>  0x0 = USB3 Port 1 DbC enabled 0x1 = USB3 Port 2 DbC enabled 0x2 = USB3 Port 3 DbC enabled 0x3 = USB3 Port 4 DbC enabled 0x4 = USB3 Port 5 DbC enabled 0x5 = USB3 Port 6 DbC enabled 0xff = No USB3 ports are assigned to DbC  All other values are Reserved	This setting determines which USB3 port goes to the target USB2 ports connector for Early DbC debugging.	Yes
	7:0	<b>USB2 DbC port enable:</b>  0x0 = USB2 Port 1 DbC enabled 0x1 = USB2 Port 2 DbC enabled 0x2 = USB2 Port 3 DbC enabled 0x3 = USB2 Port 4 DbC enabled 0x4 = USB2 Port 5 DbC enabled 0x5 = USB2 Port 6 DbC enabled 0x6 = USB2 Port 7 DbC enabled 0x7 = USB2 Port 8 DbC enabled 0x8 = USB2 Port 9 DbC enabled 0x9 = USB2 Port 10 DbC enabled 0xff = No USB2 ports are assigned to DbC  All other values are Reserved	This setting determines which USB2 ports are enabled for Early DbC debugging.	Yes



# 10 Configuration Dependencies

## 10.1 Descriptor Configuration Setting Enabling Dependencies

This chapter outlines the descriptor configuration dependencies for enabling Cannonlake Hardware I/O, Bus and GPIO components.

### 10.1.1 High Speed IO (HSIO) Port Enabling

Below diagram provides better illustration on HSIO muxing and next table shows how to enable each mux functionality on HSIO lane.

**Note:** Refer to EDS for exact number HSIO lane# supported. Some SKUs may have less HSIO lane. To get a full understanding on HSIO lane muxing architecture refer to the PCH EDS.

**Note:** GbE enabling is only allowed at the HSIO lanes shown in the diagram one at a time.

**Note:** SATA #1 is only allowed at HSIO Lanes shown in the diagram one at a time.

Table 10-1. Cannonlake-Y Flex I/O Map

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	UFS	UFS	GbE	GbE	SATA 0	SATA 1	GbE	GbE
Intel® RST Support	No Support				No Support				Yes				Yes	



Table 10-2. Canonlake / Coffeelake-U Flex I/O Map

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
							UFS	UFS								
							GbE	GbE								

The table below gives examples of how to enable each mux functionality on the HSIO lanes:

Table 10-3. HSIO Lane Muxing Selection (Sheet 1 of 3)

HSIO Lane (Port#)	Strap Offset (value)	Description
Lane 0 (USB P1)	FPSBA + FAh[1:0] = 0x0	USB3 / PCIe Combo Port 0 (PCIe_USB3_P0_Flex)
	FPSBA + 020h[0] = 0x0	Straps to decide XHCI Port 0 Ownership between XHCI/PCIe/CSI
Lane 0 (PCIe P1)	FPSBA + FAh[1:0] = 0x1	USB3 / PCIe Combo Port 0 (PCIe_USB3_P0_Flex)
	FPSBA + 020h[0] = 0x1	Straps to decide XHCI Port 0 Ownership between XHCI/PCIe/CSI
Lane 1 (USB P2)	FPSBA + FAh[3:2] = 0x0	USB3 / PCIe Combo Port 1 (PCIe_USB3_P0_Flex)
	FPSBA + 020h[1] = 0x0	Straps to decide XHCI Port 1 Ownership between XHCI/PCIe/CSI



Table 10-3. HSIO Lane Muxing Selection (Sheet 2 of 3)

HSIO Lane (Port#)	Strap Offset (value)	Description
Lane 1 (PCIe P2)	FPSBA + FAh[3:2] = 0x1	USB3 / PCIe Combo Port 1 (PCIE_USB3_P0_Flex)
	FPSBA + 020h[1] = 0x1	Straps to decide XHCI Port 1 Ownership between XHCI/PCIe/CSI
Lane 2 (USB P3)	FPSBA + FAh[5:4] = 0x0	USB3 / PCIe Combo Port 2 (PCIE_USB3_P0_Flex)
	FPSBA + 020h[2] = 0x0	Straps to decide XHCI Port 2 Ownership between XHCI/PCIe/CSI
Lane 2 (PCIe P3)	FPSBA + FAh[5:4] = 0x1	USB3 / PCIe Combo Port 2 (PCIE_USB3_P0_Flex)
	FPSBA + 020h[2] = 0x1	Straps to decide XHCI Port 2 Ownership between XHCI/PCIe/CSI
Lane 3 (USB P4)	FPSBA + FAh[7:6] = 0x0	USB3 / PCIe Combo Port 3 (PCIE_USB3_P0_Flex)
	FPSBA + 020h[3] = 0x0	Straps to decide XHCI Port 3 Ownership between XHCI/PCIe/CSI
Lane 3 (PCIe P4)	FPSBA + FAh[7:6] = 0x1	USB3 / PCIe Combo Port 3 (PCIE_USB3_P0_Flex)
	FPSBA + 020h[3] = 0x1	Straps to decide XHCI Port 3 Ownership between XHCI/PCIe/CSI
Lane 4 (USB P5)	FPSBA + FFh[5:4] = 0x0	USB3 / PCIe Combo Port 3 (PCIE_USB3_P0_Flex)
	FPSBA + 020h[4] = 0x0	Straps to decide XHCI Port 3 Ownership between XHCI/PCIe/CSI
Lane 4 (PCIe P5)	FPSBA + FFh[5:4] = 0x1	USB3 / PCIe Combo Port 3 (PCIE_USB3_P0_Flex)
	FPSBA + 020h[4] = 0x1	Straps to decide XHCI Port 3 Ownership between XHCI/PCIe/CSI
Lane 5 (USB P6)	FPSBA + FFh[7:6] = 0x0	USB3 / PCIe Combo Port 3 (PCIE_USB3_P0_Flex)
	FPSBA + 020h[5] = 0x0	Straps to decide XHCI Port 3 Ownership between XHCI/PCIe/CSI
Lane 5 (PCIe P6)	FPSBA + FFh[7:6] = 0x1	USB3 / PCIe Combo Port 3 (PCIE_USB3_P0_Flex)
	FPSBA + 020h[5] = 0x1	Straps to decide XHCI Port 3 Ownership between XHCI/PCIe/CSI
Lane 6 (PCIe P1)	No muxing	
Lane 7 (PCIe P8)	No muxing	
Lane 8 (PCIe P9)	No muxing	
Lane 9 (PCIe P10)	No muxing	
Lane 10 (PCIe P11)	FPSBA + F5h[1:0] = 0x1	SATA / PCIe Combo Port 0 Strap
	FPSBA + 104h [1:0] = 0x1	SATA / PCIe Select for Port 0
	FPSBA + 04h[1:0] = 0x1	SATA / PCIe GP Select for Port 1
Lane 10 (SATA P0)	FPSBA + F5h[1:0] = 0x0	SATA / PCIe Combo Port 0 Strap
	FPSBA + 104h [1:0] = 0x0	SATA / PCIe Select for Port 0
	FPSBA + 04h[1:0] = 0x0	SATA / PCIe GP Select for Port 1



Table 10-3. HSIO Lane Muxing Selection (Sheet 3 of 3)

HSIO Lane (Port#)	Strap Offset (value)	Description
Lane 11 (PCIe P12)	FPSBA + F5h[3:2] = 0x1	SATA /PCIe Combo Port 1 Strap
	FPSBA + 104h [3:2] = 0x1	SATA / PCIe Select for Port 1
	FPSBA + 04h[3:2] = 0x1	SATA / PCIe GP Select for Port 1
Lane 11 (SATA P1) <b>Note:</b> If Lane 12 is configured for SATA Lane 15 must be configured as PCIe.	FPSBA + F5h[3:2] = 0x0	SATA /PCIe Combo Port 1 Strap
	FPSBA + 104h [3:2] = 0x0	SATA / PCIe Select for Port 1
	FPSBA + 04h[3:2] = 0x0	SATA / PCIe GP Select for Port 1
Lane 12 (PCIe P13)	No muxing	
Lane 13 (PCIe P14)	No muxing	
Lane 14 (PCIe P15) <b>Canonlake / Coffeelake-U Only</b>	FPSBA + F5h[5:4] = 0x1	SATA /PCIe SATA Combo Port 2 Strap
	FPSBA + 104h [3:2] = 0x1	SATA / PCIe Select for Port 1
	FPSBA + 04h[3:2] = 0x1	SATA / PCIe GP Select for Port 1
Lane 14 (SATA P1) <b>Canonlake / Coffeelake-U Only</b> <b>Note:</b> If Lane 15 is configured for SATA Lane 12 must be configured as PCIe.	FPSBA + F5h[5:4] = 0x0	SATA /PCIe SATA Combo Port 2 Strap
	FPSBA + 104h [3:2] = 0x0	SATA / PCIe Select for Port 1
	FPSBA + 04h[3:2] = 0x0	SATA / PCIe GP Select for Port 1
Lane 15 (PCIe P16) <b>Canonlake / Coffeelake-U Only</b>	FPSBA + F8h[1:0] = 0x1	SATA /PCIe SATA Combo Port 3 Strap
	FPSBA + 104h[5:4] = 0x1	SATA / PCIe Select for Port 2
	FPSBA + 04h[5:4] = 0x1	SATA / PCIe GP Select for Port 2
Lane 15 (SATA P2) <b>Canonlake / Coffeelake-U Only</b>	FPSBA + F8h[1:0] = 0x0	SATA /PCIe SATA Combo Port 3 Strap
	FPSBA + 104h[5:4] = 0x0	SATA / PCIe Select for Port 2
	FPSBA + 04h[5:4] = 0x0	SATA / PCIe GP Select for Port 2

### 10.1.1.1 Configuring PCIe on HSIO

For PCIe Controller #1:

Recommended Steps	Straps	
1. Configure HSIO lane to be PCIe.	Refer HSIO Muxing Table	
2. Configure PCIe lane, x1, x2 or x4	FPSBA + 04Dh[4:3]	
3. Configure PCIe lane Reversal	FPSBA + 04Dh[2]	

For PCIe Controller #2:

Recommended Steps	Straps	
1. Configure HSIO lane to be PCIe.	Refer HSIO Muxing Table	
2. Configure PCIe lane, x1, x2 or x4	FPSBA + 055h[4:3]	
3. Configure PCIe lane Reversal	FPSBA + 055h[2]	

For PCIe Controller #3:

Recommended Steps	Straps	
1. Configure HSIO lane to be PCIe.	Refer HSIO Muxing Table	
2. Configure PCIe lane, x1, x2 or x4	FPSBA + 05Dh[4:3]	



Recommended Steps	Straps	
3. Configure PCIe lane Reversal	FPSBA + 05Dh[2]	

For PCIe Controller #4:

Recommended Steps	Straps	
1. Configure HSIO lane to be PCIe.	Refer HSIO Muxing Table	
2. Configure PCIe lane, x1, x2 or x4	FPSBA + 065h[4:3]	
3. Configure PCIe lane Reversal	FPSBA + 065h[2]	

### 10.1.1.2 Configure Intel® RST on PCIe

Configure Intel RST on PCIe Controller #1:

Recommended Steps	Straps	
1. Configure HSIO lane to be PCIe.	Refer HSIO Muxing Table	
2. Configure PCIe lane, to Intel RST supported lane x2 or x4	FPSBA + 0C4h[1:0]	00 - NAND Cycle Router A1 configured for PCIe NAND x1 01 - NAND Cycle Router A1 configured for PCIe NAND x2 10 - NAND Cycle Router A1 configured for PCIe NAND x4
	FPSBA + 091h[1:0]	CFG1x4, 2'b11 CFG2x2, 2'b10 CFG1x22x1, 2'b01 CFG4x1, 2'b00
	FPSBA + 0C8h[1:0]	CFG1x4, 2'b11 CFG2x2, 2'b10 CFG1x22x1, 2'b01 CFG4x1, 2'b00

Configure Intel RST on PCIe Controller #2:

Recommended Steps	Straps	
1. Configure HSIO lane to be PCIe.	Refer HSIO Muxing Table	
2. Configure PCIe lane, to Intel RST supported lane x2 or x4	FPSBA + 0C4h[3:2]	00 - NAND Cycle Router A1 configured for PCIe NAND x1 01 - NAND Cycle Router A1 configured for PCIe NAND x2 10 - NAND Cycle Router A1 configured for PCIe NAND x4
	FPSBA + 0C5h[3:2]	CFG1x4, 2'b11 CFG2x2, 2'b10 CFG1x22x1, 2'b01 CFG4x1, 2'b00
	FPSBA + 0CCh[3:2]	CFG1x4, 2'b11 CFG2x2, 2'b10 CFG1x22x1, 2'b01 CFG4x1, 2'b00

Configure Intel RST on PCIe Controller #3:



Recommended Steps	Straps	
1. Configure HSIO lane to be PCIe.	Refer HSIO Muxing Table	
2. Configure PCIe lane, to Intel RST supported lane x2 or x4	FPSBA + 0C4h[5:4]	00 - NAND Cycle Router A1 configured for PCIe NAND x1 01 - NAND Cycle Router A1 configured for PCIe NAND x2 10 - NAND Cycle Router A1 configured for PCIe NAND x4
	FPSBA + 0C5h[5:4]	CFG1x4, 2'b11 CFG2x2, 2'b10 CFG1x22x1, 2'b01 CFG4x1, 2'b00
	FPSBA + 0D0h[5:4]	CFG1x4, 2'b11 CFG2x2, 2'b10 CFG1x22x1, 2'b01 CFG4x1, 2'b00



## 10.1.2 Intel® Integrated LAN Controller Enabling

If Yes:

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
0x1B4h	6:0	0x70h	GbE MAC SMBus Address
0x1B7h	0	1b	Gbe MAC SMBus Address Enable
0x1B9h	2:0	0x2h	Reserved
0x1B8h	1:0	0x3h	Reserved
0x1BCh	6:0	0x64h	GbE PHY SMBus Address
0x10Ch	4	01b	LAN PHY Power Control GDP11 Signal Configuration Note: For non-Intel Wired LAN, set to 00b
0x1F4h	6	1b	Intel® PHY Over PCI Express Enable
0x1C0h	5:3	0x1h	GBE PCIe* Port Select 000 = PORT7 001 = PORT8 010 = PORT9 011 = PORT13 100 = PORT14
0x208h	1:0	0x3h	Reserved
0x208h	7:2	0x24h	Reserved
0x209h	6:0	0x70h	Reserved
0x209h	7	0x1h	Reserved
0x20Ah	7:3	0x1h	Reserved
0x20Ah	2:0	0x2h	PHY Connection
0x20Bh	3	1b	LC SMBus add enable GbE_ADDREN
0x20Bh	2	1b	LCD SMBus add enable PHY_ADDREN
0x20Ch	2	0x1h	Reserved
?	0	0b	Intel® integrated wired LAN Enable

## 10.1.3 Intel® Wireless LAN Controller Enabling

First step, follow HSIO mux table to enable PCIe port that connect to Wireless LAN.

Set PCIe config accordingly, x1

Then set below straps.

If yes:

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
0x1B0h	0	1b	On Die CLINK Select
0x10Ch	3	0b	SLP_WLAN# / GDP29 Signal Configuration





## 10.1.4 Deep Sx Enabling Dependencies

To enable:

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
0x170h	20	1b	Deep Sx Enable
0xC14h	20	1b	DEEPSX_PLT_CFG_SS [See Descriptor Configuration Chapter <a href="#">Section 9.1</a> for details]

## 10.1.5 Intel® SMBus Enabling

To enable SMBus:

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
0x175h	0	1b	Intel® ME SMBus Enable
0x177h	6:0	User input	Intel® ME SMBus I <sup>2</sup> C Address
0x178h	6:0	User Input	Intel® ME SMBus ASD Address
0x179h	6:0	User Input	Intel® ME SMBus MCTP Address
0x17Ah	0	1b	Intel® ME SMBus I <sup>2</sup> C Address Enable. To enable = 1b
0x17Bh	0	1b	Intel® ME SMBus ASD Address Enable
0x17Ch	0	1b	Intel® ME SMBus MCTP Address Enable
0x17Eh	31:0	User input	Intel® ME SMBus Subsystem Vendor & Device ID for ASF [31:0]
0x174h	0	0b	SMBus / SMLink TCO Slave Connection
0x186h	1:0	1b	Intel® ME SMBus Frequency



### 10.1.6 SMLink0 Enabling Dependencies

To enable SMLink0:

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
0x189h	0	<b>1b</b>	SMLink0 Enable
0x19Ah	1:0	<b>11b</b>	SMLink0 Frequency

### 10.1.7 SMLink1 Enabling Dependencies

To enable SMLink1:

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
0x19Dh	0	<b>1b</b>	SMLink1 Enable
0x19Fh	6:0	<b>User input</b>	SMLink1 I <sup>2</sup> C* Target Address
0x19Eh	7:1	<b>User Input</b>	SMLink1 GP Target Address
0x1A2h	0	<b>1b</b>	SMLink1 I <sup>2</sup> C Target Address Enable
0x19Eh	0	<b>1b</b>	SMLink1 GP Target Address Enable
0x1AEh	1:0	<b>1b</b>	SMLink1 Frequency



## 10.1.8 TPM over SPI Enabling Dependencies

To enable TPM over SPI:

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
0x1F0h	0	<b>1b</b>	TPM Over SPI Bus Enable
0x13Dh	2:0	<b>110b</b>	TPM Clock Frequency 010 = 48 MHz 100 = 30 MHz 110 = 17 MHz (other value not supported)

To disable TPM over SPI:

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
0x1F0h	0	<b>0b</b>	TPM Over SPI Bus Enable

## 10.1.9 mSATA/M.2 / SATA Express Enabling

### 10.1.9.1 SATA0 / PCIe11 mSATA /M.2 / SATA Express Enabling

Port 0 if running in configurable mode for SATA0PCIE0 (e.g. mSATA/M.2 / SATA Express):

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
0x104h	1:0	<b>11b</b>	SATA / PCIe GP Select for Port 0
0x1F5h	1:0	<b>11b</b>	SATA / PCIe Combo Port 0 Strap
0x204h	1:0	<b>11b</b>	SATA / PCIe Select for Port 0
0x1FCh	0	<b>0b</b>	Polarity Select SATA / PCIe Combo Port 0 (PSCPSP_P0_STRP) When SATA0PCIE0 = '0' - PCIe Mode When SATA0PCIE0 = '1' - SATA Mode
0x206h	0	<b>0b</b>	SATA / PCIe GPIO Polarity Port 0 (SPS0) When SATA0PCIE0 = '0' - PCIe Mode When SATA0PCIE0 = '1' - SATA Mode
<b>Or</b>			
0x1FCh	0	<b>1b</b>	Polarity Select SATA / PCIe Combo Port 0 (PSCPSP_P0_STRP) When SATA0PCIE0 = '0' - SATA Mode When SATA0PCIE0 = '1' - PCIe Mode
0x206h	0	<b>1b</b>	SATA / PCIe GPIO Polarity Port 0 (SPS0) When SATA0PCIE0 = '0' - SATA Mode When SATA0PCIE0 = '1' - PCIe Mode



### 10.1.9.2 SATA1A /PCIe12 mSATA /M.2 / SATA Express Enabling

Port 1, if running in configurable mode for SATAXPCIE1 (e.g. mSATA /M.2 / SATA Express):

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
0x104h	3:2	11b	SATA / PCIe GP Select for Port 1
0x1F5h	3:2	11b	SATA / PCIe Combo Port 1 Strap
0x204h	3:2	11b	SATA / PCIe Select for Port 1
0x1FCh	1	0b	Polarity Select SATA / PCIe Combo Port 1 (PSCPSP_P1_STRP) When SATAXPCIE1 = '0' - PCIe Mode When SATAXPCIE1 = '1' -SATA Mode
0x206h	1	0b	SATA / PCIe GPIO Polarity Port 1 (SPS1) When SATAXPCIE1 = '0' - PCIe Mode When SATAXPCIE1 = '1' -SATA Mode
Or			
0x1FCh	1	1b	Polarity Select SATA / PCIe Combo Port 1 (PSCPSP_P1_STRP) When SATAXPCIE1 = '0' - SATA Mode When SATAXPCIE1 = '1' -PCIe Mode
0x206h	1	1b	SATA / PCIe GPIO Polarity Port 1 (SPS1) When SATAXPCIE1 = '0' - SATA Mode When SATAXPCIE1 = '1' -PCIe Mode

### 10.1.9.3 SATA1B / PCIe15 mSATA /M.2 / SATA Express Enabling

Port 2, if running in configurable mode for SATAXPCIE1 (e.g. mSATA /M.2 / SATA Express):

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
0x104h	3:2	11b	SATA / PCIe GP Select for Port 1
0x1F5h	5:4	11b	SATA /PCIe Combo Port 2 Strap
0x204h	3:2	11b	SATA / PCIe Select for Port 1
0x1FCh	2	0b	Polarity Select SATA / PCIe Combo Port 3 (PSCPSP_P3_STRP) When SATAXPCIE1 = '0' - PCIe Mode When SATAXPCIE1 = '1' -SATA Mode
0x206h	1	0b	SATA / PCIe GPIO Polarity Port 1 (SPS1) When SATAXPCIE1 = '0' - PCIe Mode When SATAXPCIE1 = '1' -SATA Mode
Or			
0x1FCh	3	1b	Polarity Select SATA / PCIe Combo Port 3 (PSCPSP_P3_STRP) When SATAXPCIE1 = '0' - SATA Mode When SATAXPCIE1 = '1' -PCIe Mode
0x206h	1	1b	SATA / PCIe GPIO Polarity Port 1 (SPS1) When SATAXPCIE1 = '0' - SATA Mode When SATAXPCIE1 = '1' - PCIe Mode



#### 10.1.9.4 SATA2 / PCIe16 mSATA /M.2 / SATA Express Enabling

Port 3, if running in configurable mode for SATAXPCIE2 (e.g. mSATA /M.2 / SATA Express):

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
0x104h	5:4	<b>11b</b>	SATA / PCIe GP Select for Port 2
0x1F8h	1:0	<b>11b</b>	SATA / PCIe Combo Port 3 Strap
0x204h	5:4	<b>11b</b>	SATA / PCIe Select for Port 2
0x1FCh	3	<b>0b</b>	Polarity Select SATA / PCIe Combo Port 2 (PSCPSP_P4_STRP) When SATAXPCIE2 = '0' - PCIe Mode When SATAXPCIE2 = '1' - SATA Mode
0x206h	2	<b>0b</b>	SATA / PCIe GPIO Polarity Port 2 (SPS2) When SATAXPCIE2 = '0' - PCIe Mode When SATAXPCIE2 = '1' - SATA Mode
<b>Or</b>			
0x1FCh	4	<b>1b</b>	Polarity Select SATA / PCIe Combo Port 2 (PSCPSP_P4_STRP) When SATAXPCIE2 = '0' - SATA Mode When SATAXPCIE2 = '1' - PCIe Mode
0x206h	2	<b>1b</b>	SATA / PCIe GPIO Polarity Port 2 (SPS2) When SATAXPCIE2 = '0' - SATA Mode When SATAXPCIE2 = '1' - PCIe Mode



## 10.1.10 USB 3.1 Gen1 / 3.1 Gen2 Enabling Dependencies

### 10.1.10.1 USB3 / PCIe Combo Port 0:

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
Port 1 Configured as USB 3.1			
0x1FAh	1:0	00b	Port 1 configured as USB3
0x120h	0	0b	Port 1 configured as XHCI
Port 1 Configured as PCIe #1			
0x1FAh	1:0	01b	Port 1 configured as PCIe
0x120h	0	1b	Port 1 configured as Non-XHCI

### 10.1.10.2 USB3 / PCIe Combo Port 1:

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
Port 2 Configured as USB 3.1			
0x1FAh	3:2	00b	Port 2 configured as USB3
0x120h	1	0b	Port 2 configured as XHCI
Port 2 Configured as PCIe #2			
0x1FAh	3:2	01b	Port 2 configured as PCIe
0x120h	1	1b	Port 2 configured as Non-XHCI

### 10.1.10.3 USB3 / PCIe Combo Port 2:

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
Port 3 Configured as USB 3.1			
0x1FAh	5:4	00b	Port 3 configured as USB3
0x120h	2	0b	Port 3 configured as XHCI
Port 3 Configured as PCIe #3			
0x1FAh	5:4	01b	Port 3 configured as PCIe
0x120h	2	1b	Port 3 configured as Non-XHCI

### 10.1.10.4 USB3 / PCIe Combo Port 3:

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
Port 4 Configured as USB 3.1			
0x1FAh	7:6	00b	Port 4 configured as USB3
0x120h	3	0b	Port 4 configured as XHCI
Port 4 Configured as PCIe #4			
0x1FAh	7:6	01b	Port 4 configured as PCIe
0x120h	3	1b	Port 4 configured as Non-XHCI



#### 10.1.10.5 USB3 / PCIe Combo Port 4:

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
Port 5 Configured as USB 3.1			
0x1FAh	5:4	00b	Port 5 configured as USB3
0x120h	4	0b	Port 5 configured as XHCI
Port 5 Configured as PCIe #4			
0x1FAh	5:4	01b	Port 5 configured as PCIe
0x120h	4	1b	Port 5 configured as Non-XHCI

#### 10.1.10.6 USB3 / PCIe Combo Port 5:

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
Port 6 Configured as USB 3.1			
0x1FAh	7:6	00b	Port 6 configured as USB3
0x120h	5	0b	Port 6 configured as XHCI
Port 6 Configured as PCIe #4			
0x1FAh	7:6	01b	Port 6 configured as PCIe
0x120h	5	1b	Port 6 configured as Non-XHCI



### 10.1.10.7 USB 3.1 Port 1 Gen1/Gen2 Speed Select/Initialization:

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
<b>USB3 Port 1 Configured as USB 3.1 Gen1</b>			
0x122h	0	1b	Port 1 Speed Select set to Gen1 speed
<b>USB 3 Port 1 Initialization Speed</b>			
0x123h	0	N/A	Port 1 Initialize at Gen1 speed then switch over to Gen2 after LBPM
<b>Or</b>			
0x123h	0	N/A	Port 1 Initialize at Gen2
<b>USB3 Port 1 Configured as USB 3.1 Gen2</b>			
0x122h	0	0b	Port 1 Speed Select set to Gen2 speed
<b>USB 3 Port 1 Initialization Speed</b>			
0x123h	0	1b	Port 1 Initialize at Gen1 speed then switch over to Gen2 after LBPM
<b>Or</b>			
0x123h	0	0b	Port 1 Initialize at Gen2

### 10.1.10.8 USB 3.1 Port 2 Gen1/Gen2 Speed Select/Initialization:

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
<b>USB3 Port 1 Configured as USB 3.1 Gen1</b>			
0x122h	1	1b	Port 1 Speed Select set to Gen1 speed
<b>USB 3 Port 1 Initialization Speed</b>			
0x123h	1	N/A	Port 1 Initialize at Gen1 speed then switch over to Gen2 after LBPM
<b>Or</b>			
0x123h	1	N/A	Port 1 Initialize at Gen2
<b>USB3 Port 1 Configured as USB 3.1 Gen2</b>			
0x122h	1	0b	Port 1 Speed Select set to Gen2 speed
<b>USB 3 Port 1 Initialization Speed</b>			
0x123h	1	1b	Port 1 Initialize at Gen1 speed then switch over to Gen2 after LBPM
<b>Or</b>			
0x123h	1	0b	Port 1 Initialize at Gen2





#### 10.1.10.9 USB 3.1 Port 3 Gen1/Gen2 Speed Select/Initialization:

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
<b>USB3 Port 1 Configured as USB 3.1 Gen1</b>			
0x122h	2	1b	Port 1 Speed Select set to Gen1 speed
<b>USB 3 Port 1 Initialization Speed</b>			
0x123h	2	N/A	Port 1 Initialize at Gen1 speed then switch over to Gen2 after LBPM
<b>Or</b>			
0x123h	2	N/A	Port 1 Initialize at Gen2
<b>USB3 Port 1 Configured as USB 3.1 Gen2</b>			
0x122h	2	0b	Port 1 Speed Select set to Gen2 speed
<b>USB 3 Port 1 Initialization Speed</b>			
0x123h	2	1b	Port 1 Initialize at Gen1 speed then switch over to Gen2 after LBPM
<b>Or</b>			
0x123h	2	0b	Port 1 Initialize at Gen2

#### 10.1.10.10 USB 3.1 Port 4 Gen1/Gen2 Speed Select/Initialization:

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
<b>USB3 Port 1 Configured as USB 3.1 Gen1</b>			
0x122h	3	1b	Port 1 Speed Select set to Gen1 speed
<b>USB 3 Port 1 Initialization Speed</b>			
0x123h	3	N/A	Port 1 Initialize at Gen1 speed then switch over to Gen2 after LBPM
<b>Or</b>			
0x123h	3	N/A	Port 1 Initialize at Gen2
<b>USB3 Port 1 Configured as USB 3.1 Gen2</b>			
0x122h	3	0b	Port 1 Speed Select set to Gen2 speed
<b>USB 3 Port 1 Initialization Speed</b>			
0x123h	3	1b	Port 1 Initialize at Gen1 speed then switch over to Gen2 after LBPM
<b>Or</b>			
0x123h	3	0b	Port 1 Initialize at Gen2



#### 10.1.10.11 USB 3.1 Port 5 Gen1/Gen2 Speed Select/Initialization:

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
<b>USB3 Port 1 Configured as USB 3.1 Gen1</b>			
0x122h	4	<b>1b</b>	Port 1 Speed Select set to Gen1 speed
<b>USB 3 Port 1 Initialization Speed</b>			
0x123h	4	<b>N/A</b>	Port 1 Initialize at Gen1 speed then switch over to Gen2 after LBPM
<b>Or</b>			
0x123h	4	<b>N/A</b>	Port 1 Initialize at Gen2
<b>USB3 Port 1 Configured as USB 3.1 Gen2</b>			
0x122h	4	<b>0b</b>	Port 1 Speed Select set to Gen2 speed
<b>USB 3 Port 1 Initialization Speed</b>			
0x123h	4	<b>1b</b>	Port 1 Initialize at Gen1 speed then switch over to Gen2 after LBPM
<b>Or</b>			
0x123h	4	<b>0b</b>	Port 1 Initialize at Gen2

#### 10.1.10.12 USB 3.1 Port 6 Gen1/Gen2 Speed Select/Initialization:

Offset from 0	Bits	Required Value	Descriptor Configuration Parameter
<b>USB3 Port 1 Configured as USB 3.1 Gen1</b>			
0x122h	5	<b>1b</b>	Port 1 Speed Select set to Gen1 speed
<b>USB 3 Port 1 Initialization Speed</b>			
0x123h	5	<b>N/A</b>	Port 1 Initialize at Gen1 speed then switch over to Gen2 after LBPM
<b>Or</b>			
0x123h	5	<b>N/A</b>	Port 1 Initialize at Gen2
<b>USB3 Port 1 Configured as USB 3.1 Gen2</b>			
0x122h	5	<b>0b</b>	Port 1 Speed Select set to Gen2 speed
<b>USB 3 Port 1 Initialization Speed</b>			
0x123h	5	<b>1b</b>	Port 1 Initialize at Gen1 speed then switch over to Gen2 after LBPM
<b>Or</b>			
0x123h	5	<b>0b</b>	Port 1 Initialize at Gen2



# A FAQ and Troubleshooting

## A.1 FAQ

**Q: How do I find the Flash Programming Tool (FPT) and Flash Image Tool (FIT) for my platform?**

**A:** The aforementioned flash tools are included in the system tools directory in Intel® ME FW kit. Please ensure that you download the appropriate kit for the target platform.

Target	Platform Name In VIP	Kit Name
Cannonlake	Cannonlake Platform	Intel® Management Engine 11.X (use latest version)

**Q: How do I build an Image for my Intel PCH based platform?**

**A:** Cannonlake PCH-LP family based platforms, you can follow the appropriate instructions in the FW Bringup Guide which is located in the root directory of the appropriate Intel® ME KIT.

**Q: Is my flash part supported by the Flash Programming Tool (FPT)? How can I add support for a new flash to FPT?**

**A:** Look at fparts.txt to see if the intended flash part is present. If the intended flash part meets the guidelines defined in the *Cannonlake PCH-LP Family External Design Specification (EDS)*, Intel® Management Engine (Intel® ME) Firmware SPI Flash Requirements and support may be added to FPT by adding an entry for the part into the Fparts.txt file.

**Q: Is my flash part supported by Intel® ME Firmware? How can I add support for a new flash to Intel® ME Firmware?**

**A:** As long as the SPI flash devices meets the requirements defined in the *Cannonlake PCH-LP Family External Design Specification (EDS)*, support may be added for the device. BIOS will have to set up the Host VSCC registers. The Intel Management Engine VSCC table in the descriptor will also have to be set up in order to get Intel® ME firmware to work.

Adding support does not imply validation or guarantee a flash part will work. Platform designers/integrators will have to validate all flash parts with their platforms to ensure full functionality and reliability.

**Q: Do I have to use SFDP enabled SPI flash parts?**

**A:** Yes you will need to use SFDP enabled SPI flash parts regardless of using the VSCC table entries Cannonlake does not support VSCC only SPI flash parts.

**Q: Why does FPT/verify fail for my system even when I wrote nothing to flash?**

**A:** Intel® ME Firmware performs periodic writes to SPI flash when it is active. Due to this the ME region may not match the source file. There are also other system activities beside the Intel® ME that can change the data on the flash vs the original image. For example, the GbE check sum is updated on flash part whenever the value is incorrect.



**Q: How can I overwrite the descriptor when FPT does not have write access? How can I overwrite a region that is locked down by descriptor protections? How do I write to flash space that is not defined by the descriptor?**

**A:** By asserting HDA\_SDO (flash descriptor override strap) low on the rising edge of PWROK, you can read, write and erase all of SPI flash space regardless of descriptor protections. Any protections imposed by BIOS or directly to the SPI flash part still apply. This should only be used in debug or manufacturing environments. End customers should **NOT** receive systems with this strap engaged.

**Q: I have two flash parts installed on the board. Why does fpt /i only show one flash part?**

**A:** Cannonlake PCH-LP will not recognize the second SPI flash part unless it is in descriptor mode and the Component section of the descriptor properly describes the flash. Another possibility is that you have two different flash parts and the second flash part is not defined in fparts.txt.

## A.2 Troubleshooting

**Q: I'm seeing the following error:**

```
Intel(R) Flash Programming Tool. Version:  x.x.x.xxxx
Copyright (c) 2007-2015, Intel Corporation. All rights reserved.
Platform: Intel(R) Qxx Express Chipset
Reading HSFSTS register... Flash Descriptor: Invalid

--- Flash Devices Found ---

Error: Timedout waiting for hardware to complete read operation!
      SSFSTS register: 0x00

Error: Timedout waiting for hardware to complete read operation!
      SSFSTS register: 0x00

Error: Timedout waiting for hardware to complete read operation!
      SSFSTS register: 0x00

Error: Failed to read the device ID from the flash part!
```

**A:** You may be using the wrong version of FPT. Please ensure that you are using the flash tools that were provided in the kit for the target systems.

**Q: What does following FPT error message mean?**

**Error: The host does not have write access to the target flash memory!**

**A:** In order for FPT to read or write to a given region, BIOS/Host must have read/write permissions to that target region. This access is set in the descriptor. Look closely at all the addresses defined in the output of FPT /i. If there are any gaps in flash space defined you cannot perform a full flash write. You have to update region by region. Refer to [4.3 Region Access Control](#) for more information. You may have to reflash the descriptor to get the proper access.



**Q: What does following FPT error message mean?**

**Error: Flash program registers are locked! HSFSTS[15] (FLOCKDN).**

**A:** The Flash Configuration Lock-Down (FLCOKDN) bit was set HSFS (hardware sequencing flash status register). This locks down all the program registers in the ICH. If your BIOS and descriptor do not set up Hardware Sequencing, you will have to leave this bit unset in order to use FPT. You may have to upgrade the latest version of FPT as older versions do not support Hardware Sequencing. Please refer to [Hardware Sequencing Flash Status Register](#) in the *Cannonlake PCH-LP Family External Design Specification (EDS)* for the location for the HSFS. Try reflashing the SPI device with a 3<sup>rd</sup> Party programmer. If you still see this error message, please contact your BIOS vendor to ensure that they are not setting this bit.

**Q: What does following FPT error message mean?**

**Error: There is no supported SPI flash device installed.**

**A:** See the answer to the question above: *Is my flash part supported by the Flash Programming Tool (FPT)? How can I add support for a new flash to FPT?*

If the tool correctly identifies the flash part installed and still gives an error message like:

--- Flash Devices Found ---

SPI 1234 ID:0x123456 Size: 4096KB (32768Kb)  
Device ID: 0xFFFF not supported.

**Error 405: There is no supported SPI flash device installed**

This error will result when the descriptor has two flash parts defined. Edit the image via FIT/FITC and set the number of flash components to 1.

See [6.4 Recommendations for Flash Configuration Lockdown and Vendor Component Lock Bits](#) for Opcodes required for FPT operation.

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